



May 2002  
Revised June 2011

## RP-SM304A 32-Stage Static Shift Register

### General Description

The RP-SM304A is a 32-stage parallel input/serial output shift register. A parallel load clock input (PL) enables individual JAM inputs to each of 32 stages. A Q output (D) is available from the last stage. All outputs have equal source and sink current capabilities and conform to standard "4000B" series output drive.

When the PL clock input is in the logical "1" state, data is serially shifted into the register synchronously with the negative transition of the shift clock (CLK). When the shift clock is in the logical "0" state, data is jammed into each stage of the register synchronously with the positive transition of the PL clock.

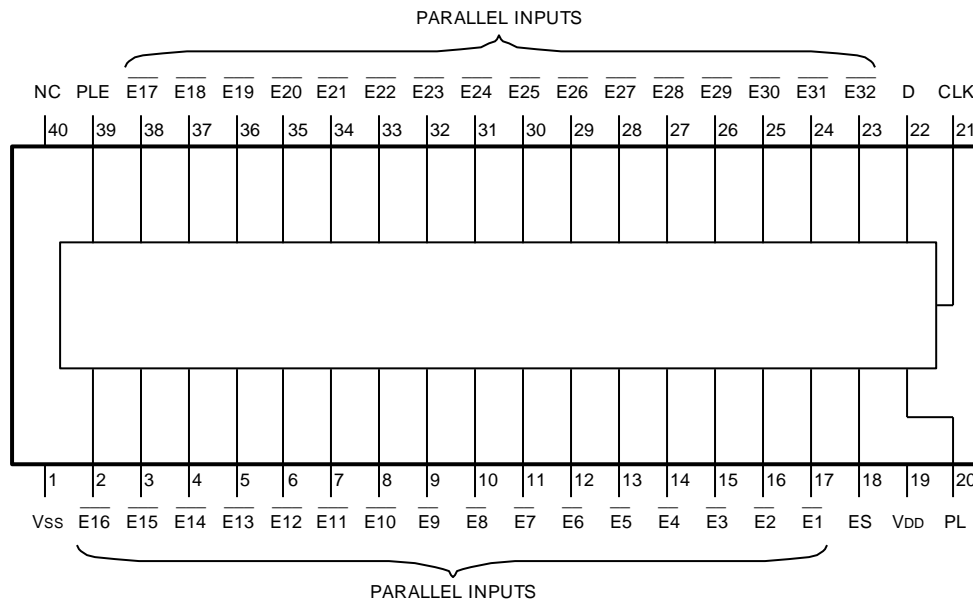
All inputs are protected against static discharge with diodes to  $V_{DD}$  and  $V_{SS}$ .

Parallel Inputs E1 through E32 are pulled high to  $V_{DD}$  with  $1M\Omega$  resistors to facilitate being driven by open-collector, open-drain, or switch contacts to ground.

### Features

- Direct replacement for Siemens SM304A for parallel-to-serial applications
- Wide supply voltage range: 3.0V to 15V
- Schmitt trigger inputs on inputs ES, PL, and CLK
- High noise immunity:  $0.45 V_{DD}$  for PLE and Parallel Inputs, and  $0.70 V_{DD}$  for inputs ES, PL, and CLK (typ)
- Low power TTL compatibility:  
Fan out of 2 driving 74L or 1 driving 74LS
- Maximum input leakage  $1\mu A$  at 15V over full temperature range

### Connection Diagram



Top View

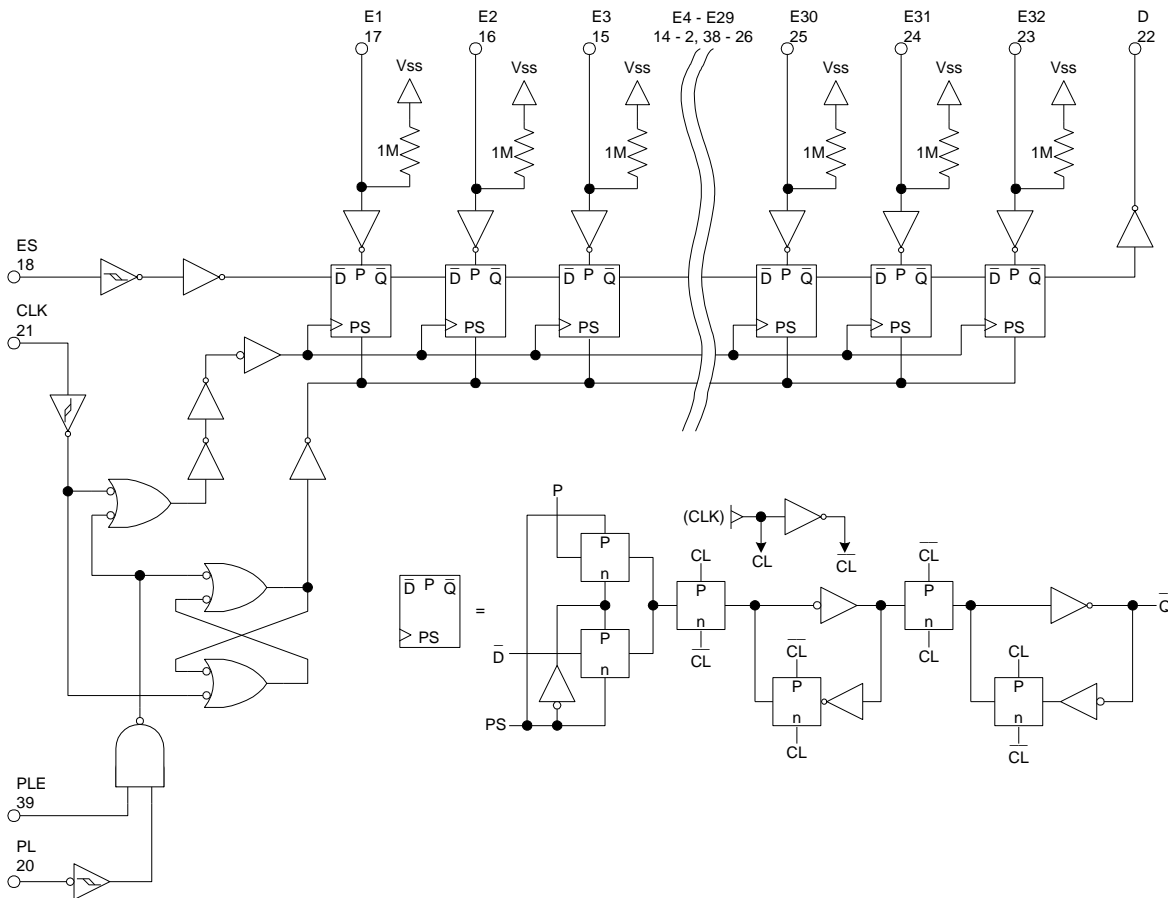
### Truth Table

CLK (Note 1)	ES	PLE	PL (Note 1)	$\overline{E1}$	$\overline{En}$	$\overline{E32}$	$Q_1$ (Internal)	$Q_n$ (Internal)	D
0	X	0	X	X	X	X	$Q_1$	$Q_n$	$Q_{32}$
0	X	X	↓	X	X	X	$Q_1$	$Q_n$	$Q_{32}$
0	X	1	↑	0	0	0	0	0	0
0	X	1	↑↑	0	0	1	0	0	1
0	X	1	↑↑↑	0	1	0	0	1	0
0	X	1	↑↑↑↑	0	1	1	0	1	1
0	X	1	↑↑↑↑↑	1	0	0	1	0	0
0	X	1	↑↑↑↑↑↑	1	0	1	1	0	1
0	X	1	↑↑↑↑↑↑↑	1	1	0	1	1	0
0	X	1	↑↑↑↑↑↑↑↑	1	1	1	1	1	1
↓	0	1	1	X	X	X	0	$Q_{n-1}$	$Q_{31}$
↑	1	1	1	X	X	X	1	$Q_{n-1}$	$Q_{31}$
↑	X	1	1	X	X	X	$Q_1$	$Q_n$	$Q_{32}$

X = Don't care case

Note 1: Level change

### Logic Diagram



### Absolute Maximum Ratings

(Note 2)

Supply Voltage ( $V_{DD}$ )	-0.3V to +18V
Input Voltage ( $V_{IN}$ )	-0.3V to $V_{DD}+0.3V$
Storage Temperature Range ( $T_S$ )	-65°C to 150°C
Power Dissipation ( $P_D$ )	500mW
Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C

### Recommended Operating Conditions

(Note 3)

Supply Voltage ( $V_{DD}$ )	3.0V to 15V
Input Voltage ( $V_{IN}$ )	0 to $V_{DD}$
Operating Temperature Range ( $T_A$ )	-55°C to +125°C

**Note 2:** "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

**Note 3:**  $V_{SS} = 0V$  unless otherwise specified.

### DC Electrical Characteristics

(Note 3)

Symbol	Parameter	Conditions	-55°C		+25°C			+125°C		Units
			Min	Max	Min	Typ	Max	Min	Max	
$I_{DD}$	Quiescent Device Current	$V_{DD} = 5V, V_{IN} = V_{DD}$ or $V_{SS}$		35		0.5	35		600	$\mu A$
		$V_{DD} = 10V, V_{IN} = V_{DD}$ or $V_{SS}$		55		0.8	55		1200	
		$V_{DD} = 15V, V_{IN} = V_{DD}$ or $V_{SS}$		95		1.2	95		2400	
$V_{OL}$	LOW Level Output Voltage	$V_{DD} = 5V, I_O < 1\mu A$		0.05		0	0.05		0.05	V
		$V_{DD} = 10V, I_O < 1\mu A$		0.05		0	0.05		0.05	
		$V_{DD} = 15V, I_O < 1\mu A$		0.05		0	0.05		0.05	
$V_{OH}$	HIGH Level Output Voltage	$V_{DD} = 5V, I_O < -1\mu A$	4.95		4.95	5		4.95		V
		$V_{DD} = 10V, I_O < -1\mu A$	9.95		9.95	10		9.95		
		$V_{DD} = 15V, I_O < -1\mu A$	14.95		14.95	15		14.95		
$V_{IL}$	LOW Level Input Voltage, PLE, E1 through E32 (Parallel Inputs)	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$		1.5		2	1.5		1.5	V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$		3.0		4	3.0		3.0	
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$		4.0		6	4.0		4.0	
$V_{IH}$	HIGH Level Input Voltage, PLE, E1 through E32 (Parallel Inputs)	$V_{DD} = 5V, V_O = 0.5V$ or $4.5V$	3.5		3.5	3		3.5		V
		$V_{DD} = 10V, V_O = 1.0V$ or $9.0V$	7.0		7.0	6		7.0		
		$V_{DD} = 15V, V_O = 1.5V$ or $13.5V$	11.0		11.0	9		11.0		
$V_{OH}$	Positive Going Threshold Voltage (Inputs ES, PL, and CLK)	$V_{DD} = 5V$	3.0	4.3	3.0	3.6	4.3	3.0	4.3	V
		$V_{DD} = 10V$	6.0	8.6	6.0	6.8	8.6	6.0	8.6	
		$V_{DD} = 15V$	9.0	12.9	9.0	10.0	12.9	9.0	12.9	
$V_{IL}$	Negative Going Threshold Voltage (Inputs ES, PL, and CLK)	$V_{DD} = 5V$	0.7	2.0	0.7	1.4	2.0	0.7	2.0	V
		$V_{DD} = 10V$	1.4	4.0	1.4	3.2	4.0	1.4	4.0	
		$V_{DD} = 15V$	2.1	6.0	2.1	5.0	6.0	2.1	6.0	
$V_{IH}$	Hysteresis Voltage (Inputs ES, PL, and CLK)	$V_{DD} = 5V$	1.0	3.6	1.0	2.2	3.6	1.0	3.6	V
		$V_{DD} = 10V$	2.0	7.2	2.0	3.6	7.2	2.0	7.2	
		$V_{DD} = 15V$	3.0	10.8	3.0	5.0	10.8	3.0	10.8	
$I_{IN}$	Input Current, E1 through E32 (Parallel Inputs)	$V_{DD} = 15V, V_{IN} = 0V$		-15.1		-15	-15.1		-16.0	$\mu A$
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		0.005	0.1		1.0	
$I_{IN}$	Input Current (All Other Inputs)	$V_{DD} = 15V, V_{IN} = 0V$		-0.1		-0.005	-0.1		-1.0	$\mu A$
		$V_{DD} = 15V, V_{IN} = 15V$		0.1		0.005	0.1		1.0	

## AC Electrical Characteristics

(Note 4)

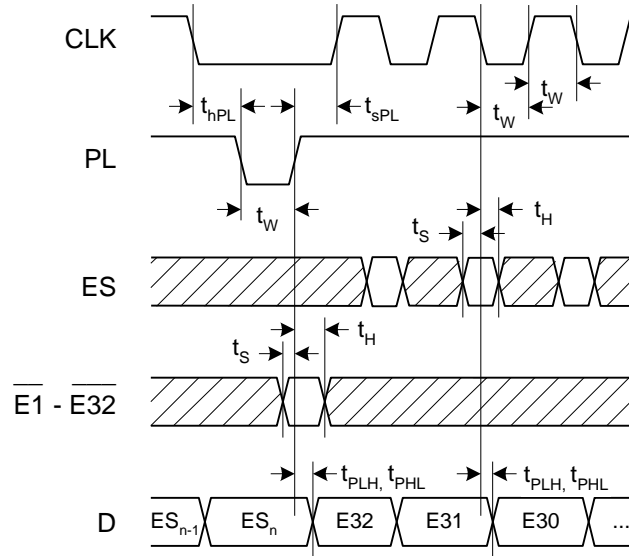
$T_A = 25^\circ\text{C}$ , input  $t_r, t_f = 20\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 200\text{k}\Omega$

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$t_{PLH}, t_{PHL}$	Propagation Delay Time, CLK $\downarrow$ to D Output	$V_{DD} = 5V$		680	1360	ns
		$V_{DD} = 10V$		340	680	
		$V_{DD} = 15V$		265	530	
	Propagation Delay Time, PL $\uparrow$ to D Output	$V_{DD} = 5V$		740	1480	ns
		$V_{DD} = 10V$		370	740	
		$V_{DD} = 15V$		290	580	
$t_{THL}, t_{TLH}$	Transition Time	$V_{DD} = 5V$		100	200	ns
		$V_{DD} = 10V$		50	100	
		$V_{DD} = 15V$		40	80	
$f_{CL}$	Maximum Input Clock Frequency	$V_{DD} = 5V$	2.8	4		MHz
		$V_{DD} = 10V$	6	12		
		$V_{DD} = 15V$	8	16		
$t_W$	Minimum Clock Pulse Width	$V_{DD} = 5V$		90	180	ns
		$V_{DD} = 10V$		40	80	
		$V_{DD} = 15V$		25	50	
$t_{sPL}, t_{hPH}$	Minimum Set-Up and Hold Time, PL Input (Ref. To CLK $\downarrow$ )	$V_{DD} = 5V$		90	180	ns
		$V_{DD} = 10V$		40	80	
		$V_{DD} = 15V$		25	50	
$t_{rCL}, t_{fCL}$	Clock Rise and Fall Time (Note 5)	$V_{DD} = 5V, 10V, 15V$			$\infty$	$\mu\text{s}$
$t_S$	Minimum Set-Up Time, ES (Serial Input), $T_H \geq 200\text{ns}$ , (Ref. To CLK $\downarrow$ )	$V_{DD} = 5V$		60	120	ns
		$V_{DD} = 10V$		40	80	
		$V_{DD} = 15V$		30	60	
	E1 through E32 (Parallel Inputs), $T_H \geq 200\text{ns}$ , (Ref. To PL $\uparrow$ )	$V_{DD} = 5V$		80	160	ns
		$V_{DD} = 10V$		40	80	
		$V_{DD} = 15V$		30	60	
$t_H$	Minimum Hold Time, ES (Serial Input), $t_S \geq 400\text{ns}$ , Ref. To CLK $\downarrow$ )	$V_{DD} = 5V$			680	ns
		$V_{DD} = 10V$			350	
		$V_{DD} = 15V$			305	
$t_H$	E1 through E32 (Parallel Inputs), $t_S \geq 400\text{ns}$ , (Ref. To PL $\uparrow$ )	$V_{DD} = 5V$			800	ns
		$V_{DD} = 10V$			410	
		$V_{DD} = 15V$			355	
$C_i$	Average Input Capacitance	Any Input		5	7.5	pF

**Note 4:** AC Parameters are guaranteed by DC correlated testing.

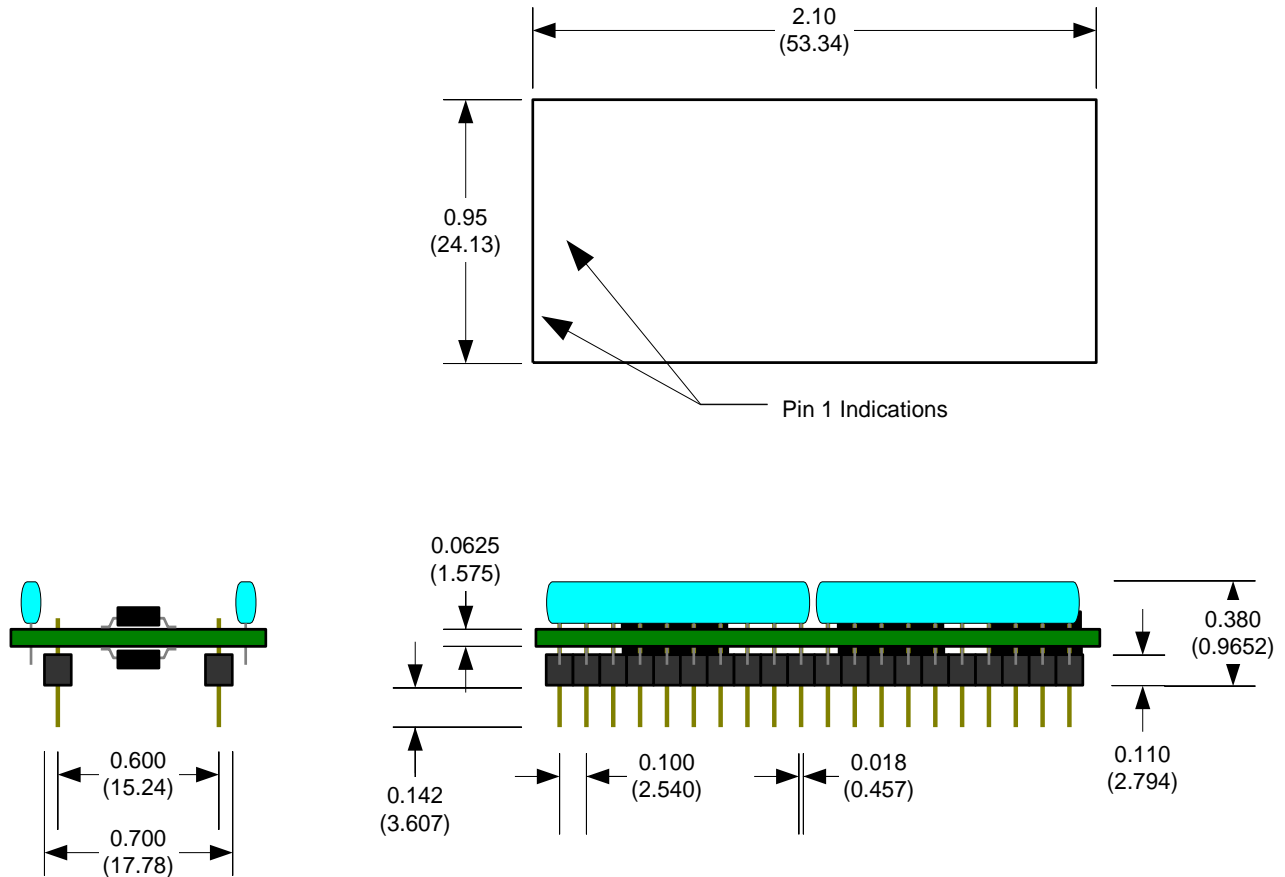
**Note 5:** Clock input is Schmitt trigger buffered.

### Timing Diagram



## Physical Dimensions

inches (millimeters) unless otherwise noted



Printed circuit board tolerance is  $\pm 0.010$  (0.254).

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