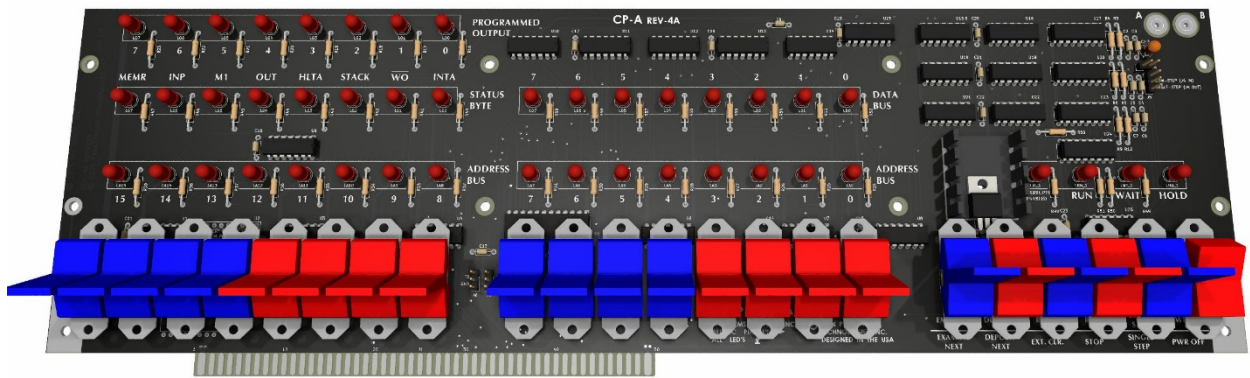


CP-A User Guide

IMSAI Series

Robert E. Weatherford
Parastream Technologies, Inc.



CONTENTS

Preface	1
Introduction	2
Related Documents.....	3
Functional Description	4
Theory of Operations	5
Parts List.....	11
Assembly Instructions.....	13
LED installation.....	13
Option Jumper Installation	14
Resistor Installation	15
IC Installation.....	15
Discrete Component Installation	16
Regulator and Heat Sink.....	16
CP-A to MPU-A Installation	17
Switch Installation.....	17
Panel Assembly.....	18
User Guide	20
Appendix	24
Changes from CP-A Rev-4	24
IEEE 696 Compatibility.....	24
Table of Figures.....	26
Schematic	27
Assembly Diagram	30
Revision History.....	31

P R E F A C E

From the president of Parastream Technologies, I would like to humbly thank you for your purchase of this classic IMSAI front panel kit. Without your continued interest in the IMSAI product line, this product would have never been made. It's been over 40 years since the last IMSAI CP-A was produced by IMSAI Manufacturing Corp. Sourcing the parts 40 years later has been difficult. Reverse-engineering most of the mechanical aspects has been quite a challenge. We took our time and used our decades of engineering experience to make this as authentic to the original as possible. I am very proud of what we came up with.

If this kit is assembled according to the Assembly Instructions, I absolutely guarantee that this front panel will fit into any stock IMSAI 8080 chassis.

Sincerely,

Robert E. Weatherford
CEO / President
Parastream Technologies, Inc.
<https://www.parastream.com>

INTRODUCTION

The IMSAI CP-A Rev-4A is a 21st century refresh of the classic IMSAI CP-A Rev-4. We started with an unbuilt IMSAI 8080 kit and meticulously reverse-engineered the mechanical parts as well as the critical PCB dimensions. We used the IMSAI CP-A schematic, Josh Bensadon's re-draft, all the related IMSAI ECOs and ECNs, and evaluated some popular aftermarket modifications. The component placement is identical to the Rev-4.

Rather than produce an exact copy of the PCB, we took the opportunity to produce a new layout to address some of the issues with the IMSAI CP-A Rev-4:

- The 120VAC traces to the power switch have been preserved, but more safely moved to the back side of the PCB and with more than twice the clearance from the main circuitry.
- The 2004 IMSAI ECO to remove UNPROT (pin 20) is a three-pin header option.
- The 2004 IMSAI ECO to use the sM1 signal to stop the CPU instead of DO5 is a three-pin header option.
- The Howard R. Bendrot modification for the "slow-stepping debugger" uses two header options and an optional 10 μ F tantalum capacitor.

In addition to these differences, all the 1970s IMSAI ECOs have been applied so no cut and jumpers are required to make the board agree with the schematic.

What didn't change is the bus directly driving the LEDs (except programmed output and data). This was a problem in the 1970s as the 8T97 and other common bus drivers did not source enough current to drive a 20mA LED. Fortunately, process improvements over the past 40 years have made the LEDs so much brighter that we can run them at very low currents down to 2mA. This puts the drive current well within the 5.2mA source drive capabilities of the bus drivers.

The mains power switching arrangement was preserved because it was done that way originally. It was made safer by routing the mains traces on the back board layer.

The IMSAI CP-A now has a silkscreen. Some users want to skip the red filter and photo mask and have nice front panel graphics on the silkscreen. Other users want the cleanest classic look possible behind the photo mask and red filter. This board strives to satisfy both groups with two board editions. The blue edition uses blue silkscreen on a black or green matte solder mask. The blue completely disappears behind the red filter, and the matte solder mask reduces reflections from ambient lighting. The white version uses white silkscreen on a gloss black solder mask which provides excellent contrast for the LEDs and graphics.

Related Documents

You may be interested in other documents in the IMSAI Series:

FUNCTIONAL DESCRIPTION

The CP-A board is the operator's panel for the IMSAI 8080 System. It includes operator switches, indicator lights and all logic necessary to operate the IMSAI 8080 System. The panel is completely self-contained and plugs into the back plane's 100 pin edge connector. With this design it is not necessary to mount the CP-A at the front of the cabinet. Instead, the board can be plugged (via an extender card) into any available slot in the back plane.¹

A full set of 16 address switches and 6 control function switches accept operator control and input. LED indicators are provided for the 16-bit address bus, the 8-bit data bus, the 8-bit status byte (control indicators for INTERRUPTS ENABLED, RUN, WAIT and 8 bits of programmed output).

The CP-A board contains the logic necessary to drive the 8 programmed output indicators and the logic needed to read an 8-bit input byte from the high-order address switches. The DATA BUS indicators are run from the bi-directional portion of the data bus (via a flat cable to the MPU board) and show data either being read or written by the 8080 processor.

The indicators on the panel are wide-angle-view light emitting diodes mounted behind a contrast-enhancing acrylic panel assembly. All indicators and switches are explicitly marked. The photographically produced labels are very clear, protected by clear acrylic, and can never wear off. Bit positions are numbered, and binary bit values are labeled for both hexadecimal and octal formats. Special labels can be easily inserted to identify special functions for the programmed output port. Switches on the panel are high-quality paddle switches and are color-coded for easy and error free use.

For situations in which it is not desired to locate the operator's panel at the cabinet front (such as use of the IMSAI 8080 as a dedicated controller), the CP-A front panel may be inserted (via extender card) into any back plane slot. In this arrangement, programs may be easily tested and debugged without time-consuming mounting and un-mounting of the front panel. For these applications, the front slot of the machine can be reserved for the parallel I/O board with its LED indicators showing through the front panel mask.

¹ The switches are included on the front panel whether it is mounted in the front of the panel or not.

THEORY OF OPERATIONS

The CP-A front panel assembly provides machine status indicators, user-controlled switches, and control functions to the IMSAI 8080 operator. The CP-A board communicates with the MPU-A microprocessor and other boards through the 8080 back plane and, additionally, connects (via 16 conductor flat cable) to the bi-directional data bus of the 8080 microprocessor. The CP-A panel uses 44 Light Emitting Diodes as front panel indicators. Many of these indicators directly correspond to signal levels on the IMSAI 8080 back plane and are driven directly from the bus with no intervening logic. Indicators in this group are the 16 Address Bus LEDs, the 8 STATUS byte LEDs, the INTERRUPT ENABLED LED, the WAIT LED, and the HOLD LED.

The 8080 microprocessor chips bi-directional data bus levels (provided by a 16-conductor cable) are displayed on the DATA bus indicators via the 74LS04 (low power Schottky hex inverter) sections. Also driven from the bi-directional bus is the 8212 8-bit latch used to drive the PROGRAMMED OUTPUT indicators. The RUN indicator is driven directly from the run/stop flip-flop (74LS107) on the CP-A Board.

The 16 ADDRESS-PROGRAMMED INPUT and ADDRESS-DATA switches allow the operator to place desired value (program, data, addresses) on the 8080's bi-directional bus. As shown on the schematic, these switches connect 74LS05 (open collector) inverters to the bus in a wired-AND configuration.

Pullup resistors on the MPU Board ensure that the bus levels are all high unless any inverter on any one of the bus lines goes low. Thus, if an inverter goes low, (this condition will be discussed shortly) the address switch can be used to put either a high or low value on that line.

The function switches provide the operator with direct control of the microprocessor. The RUN/STOP switch controls the XRDY line via the RUN/STOP flip-flop.

If the switch is set to RUN, on the next falling edge of the Phase II clock, the RUN and XRDY lines are set high. If the switch is set to STOP, the high STOP value and the Phase II clock are NANDed (U16) and this value NANDed with the DATA OUT 5 bit (fetch/status) and the PROCESSOR SYNC line. Thus, when the processor is fetching a new instruction, the RUN/STOP flip-flop will be reset, the processor X-READY line goes low, and the processor stops.

Several CP-A function switches operate by providing the 8080 with an instruction, executing the instruction, and then stopping the processor on the next cycle. The open collector 7405s

and support gating put these instructions on the 8080's bi-directional bus. The EXAMINE function uses a jump instruction (hex C3) followed by two bytes of the address selected on the front panel switches.

This operation causes the processor to jump to the selected address and then the processor is stopped during the next cycle. When stopped, the processor was reading the selected byte from memory as if it were going to execute it. Therefore, the processor stops with the desired address displayed on the address bus and the contents of that address is displayed on the data bus.

If the RUN switch is operated at this time, the processor will continue to pull the selected byte from memory and execute it.

The EXAMINE NEXT and DEPOSIT NEXT switches use similar schemes and the NO-OP (hex 00 or octal 000) instruction to increment the address.

Much of the remaining logic of the CP-A is used to sequence these commands to provide the desired functions.

The RUN/STOP flip-flop line, the SINGLE STEP line, the EXAMINE line, and the EXAMINE NEXT line are all input to an OR-gate controlling the XRDY line. (The XRDY line must be high for the processor to run. Its function is identical to the PRDY line used by the memory and I/O boards. The XRDY line is reserved for use of the front panel to avoid conflicts of two gates driving the same backplane line). During each of these functions, the processor is permitted to execute an instruction, and then is stopped in the next cycle in a manner similar to the RUN/STOP flipflop cycle described earlier.

For the SINGLE STEP function, a one-shot, triggered by the SINGLE-STEP switch, is used to produce a pulse and the trailing edge of that pulse is used to set a flip-flop which controls the SINGLE STEP line. This permits the processor to execute the present instruction. The SINGLE STEP flip-flop is reset by the occurrence of the sync pulse on the following instruction, thus causing the SINGLE STEP level to be removed and the processor to stop on the following cycle.

The EXAMINE-NEXT flip-flop is similarly controlled by the leading edge of a pulse from a one-shot driven by either the DEPOSIT NEXT or EXAMINE NEXT switch. The output of the flip-flop is used both to put the NO-OP (hex 00 or octal 000) onto the bi-directional data bus, and to provide the READY signal so that the processor will execute the instruction. It is reset by the sync pulse on the following cycle, thus stopping the processor again.

The EXAMINE function involves a 4-step sequence produced by two flip-flops arranged as a counter. The pulse produced by the EXAMINE switch's one-shot starts the counter and on the first count, the jump instruction is inserted on the data bus. On successive counts of the two-bit counter, the lower and upper address byte are inserted on the data bus in turn, and on the 4th count (that is, when the counter is back to 0), the processor is again stopped by the removal of the READY line. Thus, the EXAMINE logic provides the processor with the jump instruction and the two address bytes that the processor expects after a jump instruction and stops the processor during the fetch of the designated memory byte.

Similarly, the DEPOSIT switch, when operated, produces a pulse from the DEPOSIT one-shot which is buffered to the MEMORY WRITE line on the backplane. The leading edge of this pulse also starts a second one-shot with a much longer period which puts the data from the data switches on to the data bus for the duration of the longer pulse. The DEPOSIT one-shots are triggered either by the operation of the DEPOSIT switch or by the trailing edge of the DEPOSIT NEXT one-shot so that the DEPOSIT function will operate at the end of the EXAMINE NEXT cycle.

The 74LS27 gate in U15.5 is used to ensure that during the time the front panel is inserting any information on the bi-directional data bus, the MPU-A board's bi-directional data bus driver is also not trying to drive the bus at the same time.

The inputs to this gate are the DATA ON line, the EXAMINE NEXT line and the EXAMINE line. These are the three functions during which the front panel is transferring data or instructions to the bus.

The inputs to the 74LS05 open-collector inverter drivers are the lines NO-OP, C3, HAD, and LAD. levels are ANDed with the PDBIN signal so that information appears on the bus during the time processor is expecting to see it there.

The input port from the high order address switches is implemented simply by decoding the address FF and ANDing it with the PDBIN signal so that switch values appear on the data bus during the time that the processor is expecting information from the port FF.

The same address decode signal is ANDed with the STATUS OUT line to enable the 8212 8-bit latch which drives the PROGRAMMED OUTPUT indicators. The information on the bi-directional data bus is then latched onto the output port at the time of the processor write strobe.

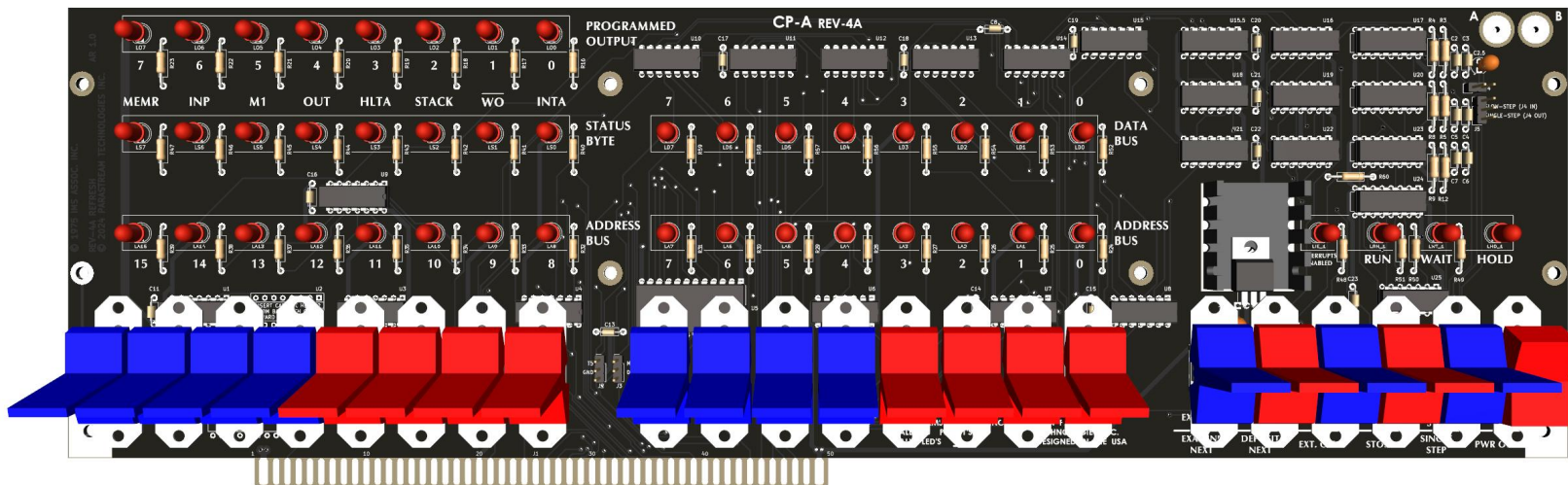
The STATUS WORD DISABLE line ($\overline{\text{SSWDSB}}$, Pin 53 backplane) is gated to ensure that no conflicts are created between the bi-directional bus drivers on the MPU and CP-A boards.

This signal is controlled by the same gating that places the high order address switch values on the data bus for a front panel (address hex FF) read.

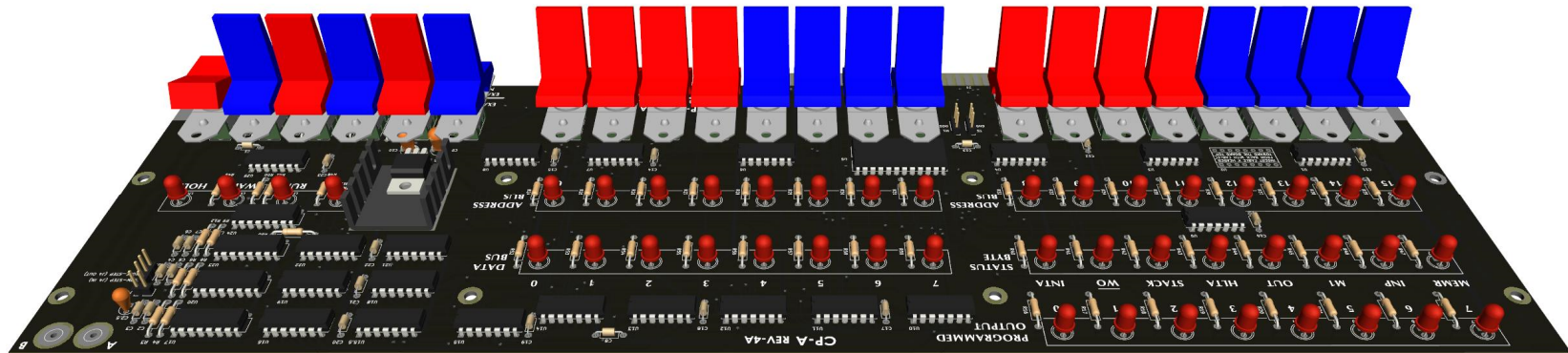
The STATUS WORD DISABLE line, Pin 53 in the backplane, is also run by the signal which puts the high order address switches onto the data bus for the port FF read instruction so that the bi-directional data bus is not being driven by the bi-directional drivers on the MPU board while the front panel is inserting the switch information on the data bus.

The RESET switch directly grounds the RESET line on the backplane which is detected by the MPU board and processed to form a RESET pulse which re-appears on the backplane as a Power On Clear.

When the RESET switch is thrown to EXTERNAL CLEAR, the switch directly grounds the EXTERNAL SWITCH line on the backplane. There is a diode between the RESET line and the EXTERNAL CLEAR line so that during a reset operation an EXTERNAL CLEAR is also generated.



CP-A REV. 4A



CP-A REV. 4A

PARTS LIST

Item	IMSAI Part #	Parastream Part #	Qty	Description
Heat Sink	16-0100002		1	Thermalloy/5106B-14
Screw	20-2203001		22	#4 × ¼" Slotted Hex Head, Self-Tapping, Type A Sheet Metal
Screw	20-3203001		2	#6 × ¼" Self-Tapping Sheet Metal
Screw	20-3302001		1	#6-32 × 5/16" Phillips Pan Head Machine
Screw	20-3916002		8	#6-32 × 1 ¼" Button Head Allen Machine, Black
Nut	21-3120001		1	#6-32 Hex
Lockwasher	21-3350001		1	#6 Internal Star Lockwasher
Spacer	21-3600001		8	#6 × ¼" White Nylon
Spacer	21-3600002		8	#6 × 7/16" White Nylon
Switch	26-1500001		8	Blue Paddle Switch, on/none/on
Switch	26-1500002		8	Red Paddle Switch, on/none/on
Switch	26-1500003		8	Red Paddle Switch, Momentary
Switch	26-1500004		8	Blue Paddle Switch, Momentary
Switch	26-1600001		8	Red Rocker Switch, on/none/on
Resistor	30-3220362		44	220Ω, ¼ Watt red/red/brown
Resistor	30-4100362	30-10032111	9	1KΩ, ¼ Watt, brown/black/red
Resistor	30-5470362		6	47KΩ, ¼ Watt, yellow/violet/black
Resistor	30-6270362		1	270KΩ, ¼ Watt, red/violet/yellow
Capacitor	32-2000110	32-10042022	2	0.001μF Disk Ceramic
Capacitor	32-2001010	32-10052022	1	0.01μF Disk Ceramic
Capacitor	32-2010010	32-10062022	18	0.1μF Disk Ceramic
Capacitor	32-2210070		1	10μF Tantalum
Capacitor	32-2233070	32-33022540	2	33μF Tantalum

Item	IMSAI Part #	Parastream Part #	Qty	Description
Diode	35-1000006		1	Signal Diode/1N914
LED	35-3000001	58-00000247	44	Light Emitting Diode/red FLV110
74LS00	36-0740002	36-10500000	2	Quad 2 Input NAND
74LS02	36-0740202	36-10500200	2	Quad 2 Input NOR
74LS04	36-0740402	36-10500400	3	Hex Inverter
74LS05	36-0740502	36-10500500	5	Hex Inverter Open Collector
74LS10	36-0741002	36-10501000	2	Triple 3 Input NAND
74LS27	36-0742702	36-10502700	1	Triple 3 Input NOR
74LS30	36-0743002	36-10503000	2	8 Input NAND
7805	36-0780501	38-00780541	1	5V Positive Volt Regulator
8212	36-0821201		1	I/O Port
74LS107	36-7410702	36-10510700	3	Dual J-K Flip Flop with Clear
74LS123	36-7412302	36-10512300	3	Dual Monostable Multivibrator, Retriggerable with Clear
74LS367	36-7436702		1	Hex Tri-State Buffer
Cable Assembly	91-0400001		1	Cable K Assembly
PC Board	N/A		1	CP-A, Rev. 4A
Plastic Panel	93-3010006		1	Clear Plastic Panel
Plastic Panel	93-3010007		1	Red Plastic Panel
Bracket	93-3010011		1	Switch Bracket
Photo Mask	93-3010015		1	
Paper Backing	93-3010016		1	

ASSEMBLY INSTRUCTIONS

- Unpack your board and check all parts against the parts lists enclosed in the package.
- If gold contacts on the edge connector appear to be corroded, use pencil eraser to remove any oxidation. NOTE: Do not use Scotchbright or any abrasive material as it will remove the gold plating.

LED installation

- For a professional appearing finished CP-A Board two items in the assembly are important: first, the mounting of the LED indicator lamps, and second, the mounting of the paddle switches. Care is necessary in the mounting of both of these items to insure evenly spaced, straight line rows of components. If they are assembled carefully, the panel will have a professional appearance second to none. If these two items are assembled haphazardly, the panel will function; however, it will have a distinctly less than workmanlike appearance.
- For maximum ease in uniform assembling, the LED indicator lamps should be installed on the board first before any other components have been installed. They should not be pushed fully against the board, but, rather, should be set up approximately $\frac{1}{8}$ inch to place them closer behind the acrylic panel mask; this provides for a greater viewing angle during panel operation. A small easy-to-make jig is extremely useful in accurate positioning of the LED indicators. This mounting aid consists of $\frac{1}{8}$ inch thick material. A piece of $\frac{1}{8}$ inch plastic, aluminum, or Masonite, or two pieces of $\frac{1}{16}$ -inch material such as Vector board or old printed circuit board make ideal jigs. A $\frac{3}{4}$ inch square piece of the $\frac{1}{8}$ inch material, or two of the $\frac{1}{16}$ -inch material should be cut and a narrow slot, such as would be produced by a hacksaw or coping saw blade, cut into one side a little bit past the center. As each light emitting diode is installed in the board, leads can be inserted through the short slot cut into this piece and then through the board and the LED should be pushed up hard against the $\frac{1}{8}$ inch piece so that its base sits flat and it will be held accurately $\frac{1}{8}$ inch away from the surface of the front panel board. The lead should be soldered from the back while someone is holding the LED against the mounting aid from the front. The mounting aid can then be slipped out from under the LED. Take care that every LED is mounted in the correct direction with the cathode down towards the 100-pin edge connector at the bottom of the board. The cathode can be recognized by its proximity to the flat side on the base of the light emitting diode.

Insert and solder each of the forty-four red LEDs at locations:

LOO through LO7
LAO through LA15
LDO through LD7
LSO through LS7
LIE, LHD, LRN, LWT

Option Jumper Installation

NOTE: The jumper areas allow the CP-A to be tailored to the requirements of your system. The PCB comes with these jumper areas default to stock CP-A Rev-4 operation. These instructions explain what each jumper does, and what the defaults are.

You may also insert standard breakaway headers into the jumper areas if you want to be able to easily change them after the CP-A has been installed. If you decide to do this, be sure to cut any default traces indicated first. Additionally, you may run into clearance problems unless you use low-profile shorting plugs.

- J2 selects the connection to the UNPROT bus pin 20.
- J3 selects the status signal used to stop the CP-A on an instruction fetch.
- J4 and J5 enable the Howard R. Bendrot modification for the “slow-stepping debugger.”

J2 selects the connection to the UNPROT bus pin 20. The default connection is to the CP-A internal “T5” line which forces all addressed memory to be unprotected. This is not recommended because it exposes an internal signal to the bus. Cut the trace on the component side between J2 pins 1 and 2. To implement the recommended configuration which prevents the CP-A from altering any existing memory protection, solder a short piece of resistor lead wire between pins 2 and 3. This will connect bus pin 20 to GND. If some other board in the system drives bus pin 20 to manage memory protection, leave all three J2 pins open.

J3 selects the status signal used to stop the CP-A on an instruction fetch. The default is to use the DO5 bus signal to detect the instruction fetch cycle. This works fine for the 8080 CPU, but other otherwise compatible CPUs such as the 8085 and Z80 do not multiplex the status byte onto the data bus. This causes erratic behavior while attempting to stop the system with the STOP switch. If you are using the CP-A with a CPU board other than

an 8080, cut the trace on the component side between pins 2 and 3 and solder a short piece of resistor lead wire between pins 1 and 2.

- J4 and J5 enable the slow-step modification. The default is that the SINGLE STEP switch operates the same way raising or lowering it. To make the switch perform a step at approximately 6 steps per second when it is raised, cut the component side trace between J5 pins 2 and 3 and solder a short piece of resistor lead wire between J4 pins 1 and 2 and J5 pins 1 and 2. Be sure to insert C2.5 in the Discrete Component Installation step.

Resistor Installation

- Insert and solder each of the forty-four 220 ohm $\frac{1}{4}$ watt resistors (red/red/brown) R16 through R59. See Assembly Diagram for location.
- Insert and solder each of the six 47K ohm $\frac{1}{4}$ watt resistors (yellow/ violet/orange) R3, R4, R5, R8, R9; and R12. See Assembly Diagram for location.
- Insert and solder one 270K ohm $\frac{1}{4}$ watt resistors (red/violet/yellow). See Assembly Diagram for location.
- Insert and solder each of the nine 1K ohm $\frac{1}{4}$ watt resistors (brown/ black/red) R2, R6, R7, R10, R11, R33 through R15, and R60. See Assembly Diagram for location.

IC Installation

- Insert and solder each of the two 74LS00 ICs at locations U14 and U25.
- Insert and solder each of the two 74LS02 ICs at locations U13 and U16.
- Insert and solder each of the three 74LS04 ICs at locations U8, U10, and U15.
- Insert and solder each of the five 74LS05 ICs at locations U1, U3, U4, U6, and U7.
- Insert and solder each of the two 74LS10 ICs at locations U11 and U12.
- Insert and solder the one 74LS27 IC at location U15.5.
- Insert and solder each of the two 74LS30 ICs at locations U9 and U21.
- Insert and solder each of the three 74LS107 ICs at locations U18, U19, and U22.
- Insert and solder each of the three 74LS123 ICs at locations U17, U20, and U23.

- Insert and solder the one 74LS367 IC at location U24.
- Insert and solder the one 8212 IC at location U5.

Discrete Component Installation

NOTE: Lead allowance on all capacitors must be long enough to allow them to be flattened (or laid down) flush on the board or chip to facilitate front panel mounting.

- Insert and solder each of the eighteen 0.1 μ F capacitors at locations C1, C2, C5, C6, C7, and C11 through C23. C2, C3, C5, C6, and C7 should be laid down.
- Insert and solder each of the two 0.001 μ F capacitors at locations C3 and C8.
- Insert and solder the one 0.01 μ f capacitor at location C4.
- If you have configured J4 and J5 to enable the slow-step modification, Insert and solder the one 10 μ f tantalum capacitor at location C2.5.
- Insert and solder the two 33 μ F 25 volt tantalum capacitors at locations C9 and C10. NOTE: Observe polarity as marked on board.
- Insert and solder the 1N914 diode at position CR1.

Regulator and Heat Sink

- Before installing heat sink bend all the heat sink fins horizontally (outward) to facilitate front panel mounting. The middle fin located on the right hand side of the board (when mounted) should be broken off or bent inward to allow space for the INTERRUPT ENABLE LED (LIE) to be seen through the front panel.
- To install the regulator and heat sink first bend the 7805 regulator leads at 90° angles to a length which allows their insertion into the hole pattern of the CP-A board. Then place the heat sink as shown in Assembly Diagram and insert regulator as described above. Use a #6 screw on the component side of the board and lock washer and nut on the solder side of the board. Tighten the screw carefully to ensure proper alignment of the heat sink to prevent shorting to adjacent traces.

CP-A to MPU-A Installation

- Using the 16-conductor ribbon cable with 16 pin 3M dual inline connector, insert one end into the hole pattern U2 from the back side of the CP-A board so that it can be soldered from the front (component side) of the CP-A board. The cable should be mounted so that it extends upward from the top of the chassis when the board is mounted.

Switch Installation

NOTE: There are three types of switches included for installation on the front panel (disregarding color). They include:

- A. One 2 position red rocker switch. This is the AC power switch.
- B. 5 momentary 3 position with spring return to center paddle switches identified by the lack of a Nipple (raised portion) on the front of the switch mounting tab.
- C. 16 2 position no spring return paddle switches.

NOTE: Temporarily plug a 100-pin edge connector onto the CP-A Board while switches are being soldered to help insure proper spacing between the PC Board and switch bracket.

- The last step is the assembly of the switches and the switch mounting bracket. Note that the front panel includes switches whether mounted in the front of the cabinet or not. The POWER/ON/OFF Rocker Switch mounts at the extreme right switch position. The Paddle Switches are provided in both two-position and center-off spring return types. The two-position switches are used for the ADDRESS-DATA and ADDRESS PROGRAMMED INPUT location while the center-off spring return are used for the Control Functions.
- When the entire row has been spaced accurately, the board should be turned over and a center switch should be soldered in place taking care that the board is not bowed towards or away from the switches. When the board is positioned correctly, there will be a small space approximately $\frac{3}{64}$ inch or slightly under $\frac{1}{16}$ inch between the bottom of the switch and the front of the front panel board. The two end switches should be similarly checked to make sure that the spacing to the board is correct and soldered in place, and then one switch each at the positions checked as to spacing from the board and soldered into place. Then the remainder of the switches can be soldered. Examine visually for solder splash or bent/unsoldered pins.

Panel Assembly

Refer to Figure 1 to see how the clear front acrylic piece, the photograph mask, the die cut paper backup and the red acrylic panel are assembled in sequence with the #6-32 x 1¼ inch button head screws.

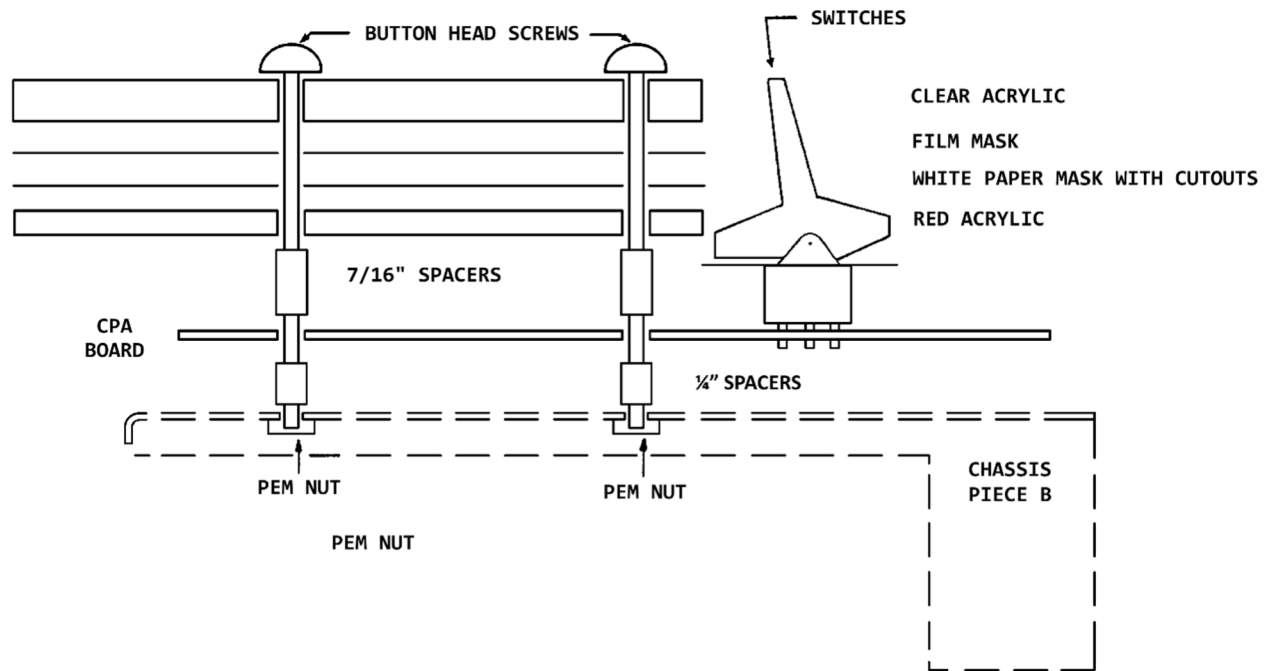


Figure 1. Panel Assembly

Both the Photographic mask and the paper backup sheet should be trimmed to size after assembly. Marks are provided on both, and they should be cut out carefully using a straight edge and a very sharp knife against a wooden cutting board. Scissors may be used if a guide line is first drawn on the sheets. The 8 holes for the assembly screws should be cut out on the mask and the paper sheet as indicated in the diagram. Then the protective paper may be removed from the two acrylic sheets and the sandwich assembled carefully. Avoid getting dust caught in between any of the pieces. A soft lint-free rag, very slightly moistened, can be an aid in cleaning any dust off of plastic or film surfaces. When the acrylic pieces, film and paper have been assembled, eight 7/16-inch spacers may be slipped over the screws and then the whole assembly inserted through the mounting holes on the CP-A board. Take care that there is no interference from any component standing too high and that the acrylic panels sit down completely on the 7/16-inch spacers against the board. Eight ¼ inch spacers can then be slipped over the screws behind the CP-A board and eight #6 nuts and lock washers can be put on to hold the sandwich together. The panel board should now be ready

to plug in and use. If the board is going to be assembled in the front location of a cabinet, to serve as a permanent front panel, the eight nuts should be removed at this time. Install the cap screws in the PEM nuts in the front panel sheet metal.

USER GUIDE

The CP-A board contains no user option jumpers or any other special connections that must be made to use the board. If the panel is mounted in the IMSAI 8080 cabinet, then the power on/off switch should be connected using a separate wire to the power supply section as described in the Power Supply documentation. If the panel board is not going to be mounted in the cabinet, then the power switch should not be connected. In this case, the power switch on the inside or on the back of the cabinet would be used for controlling power to the IMSAI 8080.

Panel installation requires a backplane slot. The panel may be plugged directly into the front slot of the mother board (with the mounting screws from the acrylic face plate assembly extending through the metal panel immediately behind and secured with lock washers and nuts) or plugged on an extender card into any location in the back plane.² The 16 pin DIP plug on the end of the flat cable must also be inserted into the corresponding socket in the upper right-hand corner of the MPU-A or MPU-B board.

Only one front panel should be plugged into the bus at any time to avoid conflicts between multiple driving sources on the same signal lines for some of the control lines between the front panel and the system bus. The front panel is now ready to operate.

The 16 ADDRESS-DATA and ADDRESS-PROGRAMMED INPUT switches are 2 position paddle switches and represent a 0 in the down position and a 1 in the up position. The switches are provided in two colors and can be arranged either in color groups of four to assist programming in hexadecimal or color groups of 3, 3 and 2, to aid in octal programming.

The low order byte of address switches serve to enter into memory either data or program instructions. These switches are labeled ADDRESS-DATA 0 through 7. Each byte of data or program that is to be entered from the front panel is set into these switches after the appropriate address has been selected and entered. The switch positions are not indicated on the indicator lights until the information is deposited in memory. At that time the information from these switches appears on the data bus. The high order byte of address switches is labeled ADDRESS-PROGRAMMED INPUT and these switches can be read by the program as input port hex FF or octal 377. The additional labels 0 through 7 are provided above these switches to assist in interpreting the switch positions when being used as an input port. The

² Switches should be included whether the front panel is mounted in the front of the cabinet or not.

position of these switches does not appear in the indicators until the input instruction from port FF is executed, during which execution time the switch positions appear on the data bus as it is being read into the 8080 processor.

The six control switches are grouped at the right end of the panel. They are center-off two-position spring-return switches with the exception of the POWER ON/OFF switch, which is a rocker type to eliminate accidental power downs. The function switches are provided in alternating colors for easy identification and to reduce operator error.

The RUN/STOP switch controls program execution. When the switch is pushed to the RUN position, a control signal is sent to the processor board and enables it to start or continue executing program instruction beginning in the location indicated at that time in the address bus lights. When the address switch is depressed to the STOP position, this enable signal is removed from the processor board at the beginning of the next instruction cycle so that the processor will stop executing during the fetch cycle for that following instruction.

When the processor is enabled to RUN, the RUN light above the RUN/STOP switch will be lit. When the processor has been stopped, the WAIT light to the right of the RUN light will be lit. During normal operation, the RUN light will be on full, and the WAIT light will be on partially, the exact amount depending on how many wait cycles are required by the memory and peripheral devices being run by the processor at the moment.

The front panel must be holding the processor in the stopped condition for the SINGLE STEP switch, the DEPOSIT/DEPOSIT NEXT switch, or the EXAMINE/EXAMINE NEXT switch to operate.

The EXAMINE/EXAMINE NEXT switch provides the facility for observing what is stored in memory in any location or for setting the program counter to any desired location to initialize program execution there.

When examining the contents of a location in memory, the 16 address switches are used to enter the 16-bit address. This 16-bit address is - normally said to be divided into two 8-bit sections labeled high order and low order. The high order address is on the left hand side of the panel, and the low order address is in the center. The low order byte contains bits 0 through 7 and the high order byte contains bits 8 through 15. When only a small amount of memory is being used the high order bits are normally 0 and the switches must be in a down position, unless the address jumper selection on the memory board is wired otherwise.

When the EXAMINE switch is actuated, the processor jumps to the address location set in the 16 address switches and is stopped during the fetch cycle out of that memory location.

At that time, the address bus indicators will show the address set in the 16 address switches and the data bus indicators will show the contents of that memory location. Any additional locations in memory may be observed by setting the 16 address switches to that desired address and actuating the EXAMINE switch again. When the EXAMINE NEXT switch is actuated, the address shown in the address bus indicators is incremented by 1 and the contents of that following memory location are displayed on the data bus lights. Thus, a program or data would normally be checked by setting the first address in the address switches and actuating the EXAMINE switch to see the first byte, and thereafter actuating the EXAMINE NEXT position to observe each succeeding byte of data or program.

The DEPOSIT/DEPOSIT NEXT switch is similar in its operation but provides for changing the data or program stored in the memory. When the switch is actuated to the DEPOSIT position, the values of the lower address byte switches, that is, bits 0 through 7 labeled Address-Data, are deposited into the address currently being indicated on the 16 address bus indicators. After the DEPOSIT switch is actuated, the data will appear on the data bus indicators. If the data was incorrect because the switches were set wrong, the switches can be changed, the DEPOSIT switch actuated again, and the new values will be deposited to memory in that same location.

When the DEPOSIT NEXT position is actuated, the address currently appearing in the 16 address bus indicators is first incremented by 1 and the data present on the ADDRESS/DATA switches is deposited in that following location and will appear in the data bus. The DEPOSIT NEXT position functions the same as depressing EXAMINE NEXT to increment the address bus by 1 and then actuating DEPOSIT to deposit the ADDRESS-DATA switch positions into that location.

When the processor is stopped, instructions may be executed one at a time using the SINGLE STEP switch to the right of the RUN/STOP switch. If this switch is depressed or raised, the processor board is permitted to run one instruction, and it will stop when it is in the fetch cycle in the following instruction. Thus, repeated operations of this switch permit the programmer to step through his program one instruction at a time and follow what the machine is doing, noticing on the data bus what the fetched instruction is, and on the address bus the location from which that instruction is being fetched. For instructions requiring multiple memory accesses, for instance those with an address following in the second or third byte, each operation of the SINGLE STEP switch advances through only one part of the instruction. Thus, each byte of the instruction being read in and each byte of data being read in or out may be observed on the panel. If the slow-step modification has been done, raising the SINGLE STEP switch will step through about 6 bus cycles per second.

The RESET/EXTERNAL CLEAR switch provides the system reset functions. When depressed to the EXTERNAL CLEAR position the CLEAR signal is given to all external input/ output interface cards which are wired to be reset by this signal. When raised to the RESET position, the 8080 processor is reset. This sets the program counter to location 0 and then returns control to the processor. If the front panel is permitting the processor to run when the RESET switch is actuated, upon release of the RESET switch the processor continues execution starting at position 0. If the front panel was holding the processor in a stopped state, during the time the RESET switch was actuated, then the program counter will be set to 0. When the RESET switch is released, the processor will remain stopped and will be positioned at memory location 0.

The 8 PROGRAMMED OUTPUT indicator lights can be controlled by the program using the output instruction to port location hex FF or octal 377. When 0-bits are output into this port, the indicator lights will be turned on and where 1-bits are output into this port, indicator lights will be turned off.

The STATUS BYTE indicator lights display the condition of the status byte during the execution of that instruction. The 8 status bits included in the status byte are the Memory Read Bit, the Input Instruction Bit, the Instruction Fetch Bit, M1, the Output Instruction Bit, the Halt/Acknowledge Bit, the Stack Operation Bit, the Write Output Complement Bit, and the Interrupt Acknowledge Bit. In normal front panel operation, whenever the machine is stopped and the EXAMINE, EXAMINE NEXT, DEPOSIT, or DEPOSIT NEXT switches are being used, the MEMR, M1, and \overline{WO} , status lights should be on.

While single stepping through a program, either these or other status lights will be on as appropriate to the instruction function being executed at that moment.

For a more complete description of the functions of the status bits, reference should be made to the Intel 8080 Micro Computer Systems User's Manual. The INTERRUPT ENABLED indicator is turned on whenever the interrupts are enabled into the 8080 processor by the INTERRUPT ENABLE INSTRUCTION. This light is turned off either by an interrupt occurring and the processor acknowledging it, or by the instruction to disable interrupts. The HOLD indicator light is lit whenever a special-purpose input/output card is holding the processor to gain direct access to the memory on the system bus.

APPENDIX

Changes from CP-A Rev-4

All the 1970s IMSAI ECNs and ECOs have been applied so no cuts and jumpers are required.

A PCB silkscreen was added. The “blue” edition uses blue silkscreen on a green or black matte solder mask. The blue completely disappears behind the red filter, and the matte solder mask reduces reflections from ambient lighting. The “white” version uses white silkscreen on a gloss black solder mask which provides excellent contrast for the LEDs and graphics.

Five board jumpers were added to allow some customization of the CP-A. These jumpers are for options that have been popular aftermarket modifications over the years:

- J2 select the connection to the UNPROT bus pin 20.
- J3 selects the status signal used to stop the CP-A on an instruction fetch.
- J4 and J5 enable the Howard R. Bendrot modification for the “slow-stepping debugger.”

All 7400-series ICs have been replaced with 74LS00-series ICs. IMSAI used the 74LS00-series sparingly in the beginning as they cost more than the 7400-series. Today, the economics are reversed, so using the 74LS00-series lowers both economic and power cost.

Changing to the 74LS00-series lead to a bus drive issue with U21 driving the XRDY bus signal. The output of U21 now routes through an unused section of the 8T97 (U24-2) driver to the bus. U24 (8T97) was replaced with a 74LS367.

The 120VAC traces to the power switch have been preserved, but more safely moved to the back side of the PCB and with more than twice the clearance from the main circuitry.

IEEE 696 Compatibility

In 1983, the IEEE standardized the S-100 bus in an attempt to stop the proliferation of incompatible bus extensions used by the marketplace. One of the primary objectives of the IEEE 696 bus was to decouple it from the 8080 CPU. While the CP-A may be configured to work correctly with the 8085 and Z80 CPUs, it will not work with others that are not binary machine code compatible with the 8080.

While this means that the CP-A cannot be strictly IEEE 696 compatible, it can be made to work in systems with a compatible CPU permanent bus master.

The first problem is that the IEEE 696 assigned pin 53 to 0V. This breaks not only the CP-A, which attempts to drive it with the \overline{SSWDSB} signal, it also breaks all “old” CPU boards that use that signal to disable their bus transceivers. If your system does not have any IEEE 696 compatible boards that may also be connecting pin 53 to 0V, the best solution is to make sure that the backplane does not connect pin 53 to 0V. If this isn’t possible, the other solution is to disconnect pin 53 from the CP-A and the CPU board. This will have the side-effect of the PROGRAMMED INPUT switches being non-functional. Performing this modification will require a trace cut on the CP-A, as well as a trace cut and possibly other changes to the CPU board.

The IEEE 696 assigned pin 98 (sSTACK) to ERROR*. This may have the side-effect of making the STACK status bus light always lit unless the ERROR* line is asserted.

The IEEE 696 deprecated pin 28 (pINTE), which drives the INTERRUPTS ENABLED LED. Depending on whether the bus pin is terminated, the LED may be always lit. The 8080 is the only CPU that drives this bus pin.

Bus pin 70 is defined as 0V on the IEEE 696 bus and is correctly connected to GND in the CP-A. Bis pin 20 is also defined as 0V on the IEEE 696 bus, and you must make certain that the component side trace between J2 pins 1 and 2 has been cut, and pins 2 and 3 are jumped.

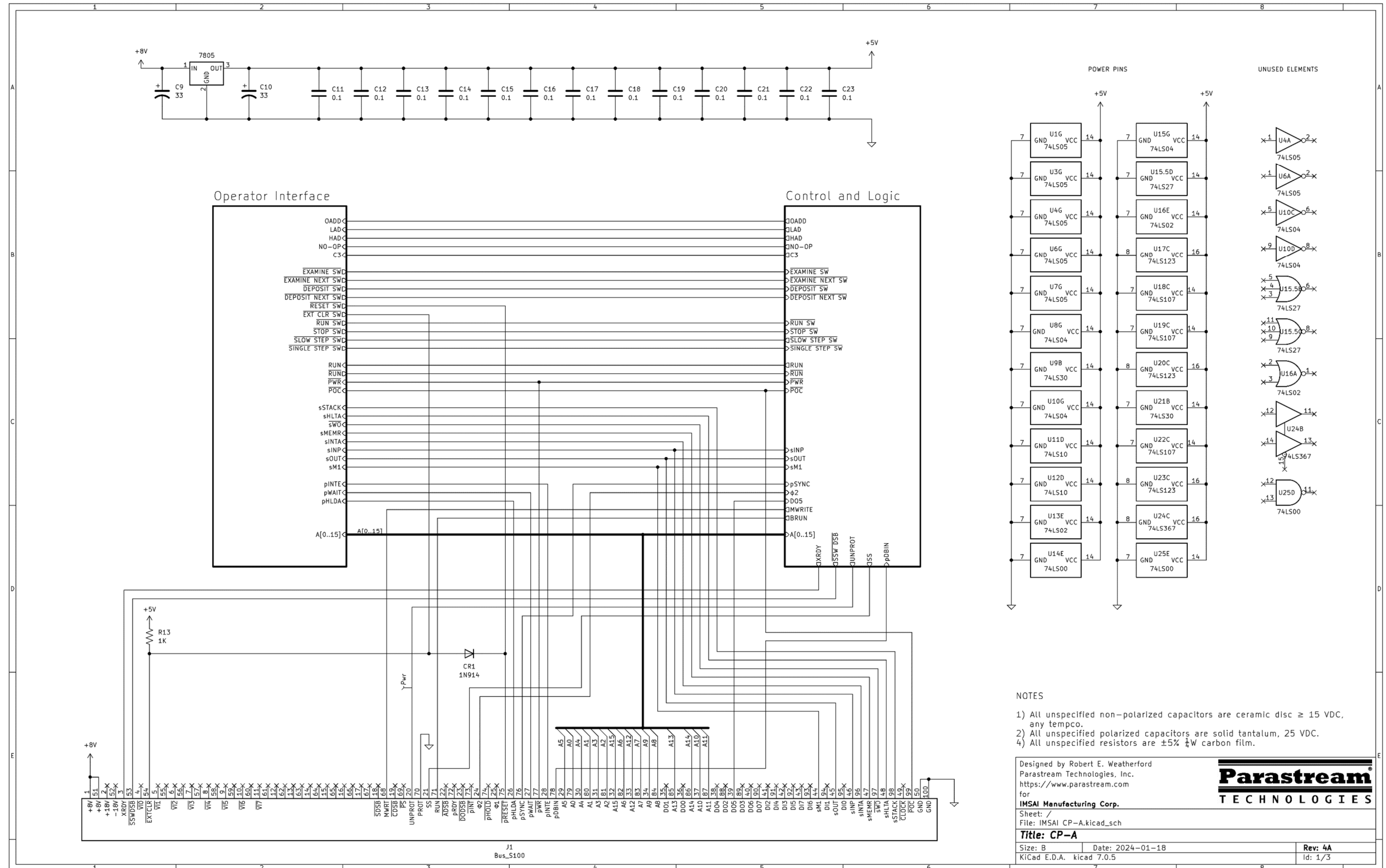
Bus pins 21 (SS) and 71 (RUN) are NDEF or RFU on the IEEE 696 bus. Backplanes should carry these signals and not affect normal CP-A operation.

With a little detective work and a compatible CPU board, you should be able to get the CP-A to work in your system.

TABLE OF FIGURES

Figure 1. Panel Assembly 18
Figure 2. Schematic Diagram, Top Sheet..... 27
Figure 3. Schematic Diagram, Operator Interface..... 28
Figure 4. Schematic Diagram, Control and Logic 29
Figure 5. Assembly Diagram..... 30

SCHEMATIC



- NOTES
- 1) All unspecified non-polarized capacitors are ceramic disc ≥ 15 VDC, any tempco.
 - 2) All unspecified polarized capacitors are solid tantalum, 25 VDC.
 - 4) All unspecified resistors are $\pm 5\%$ $\frac{1}{4}$ W carbon film.

Designed by Robert E. Weatherford
 Parastream Technologies, Inc.
<https://www.parastream.com>
 for
IMSAI Manufacturing Corp.

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 TECHNOLOGIES

Sheet: /
 File: IMSAI CP-A.kicad_sch
Title: CP-A

Size: B	Date: 2024-01-18	Rev: 4A
KiCad E.D.A. kicad 7.0.5		Id: 1/3

Figure 2. Schematic Diagram, Top Sheet

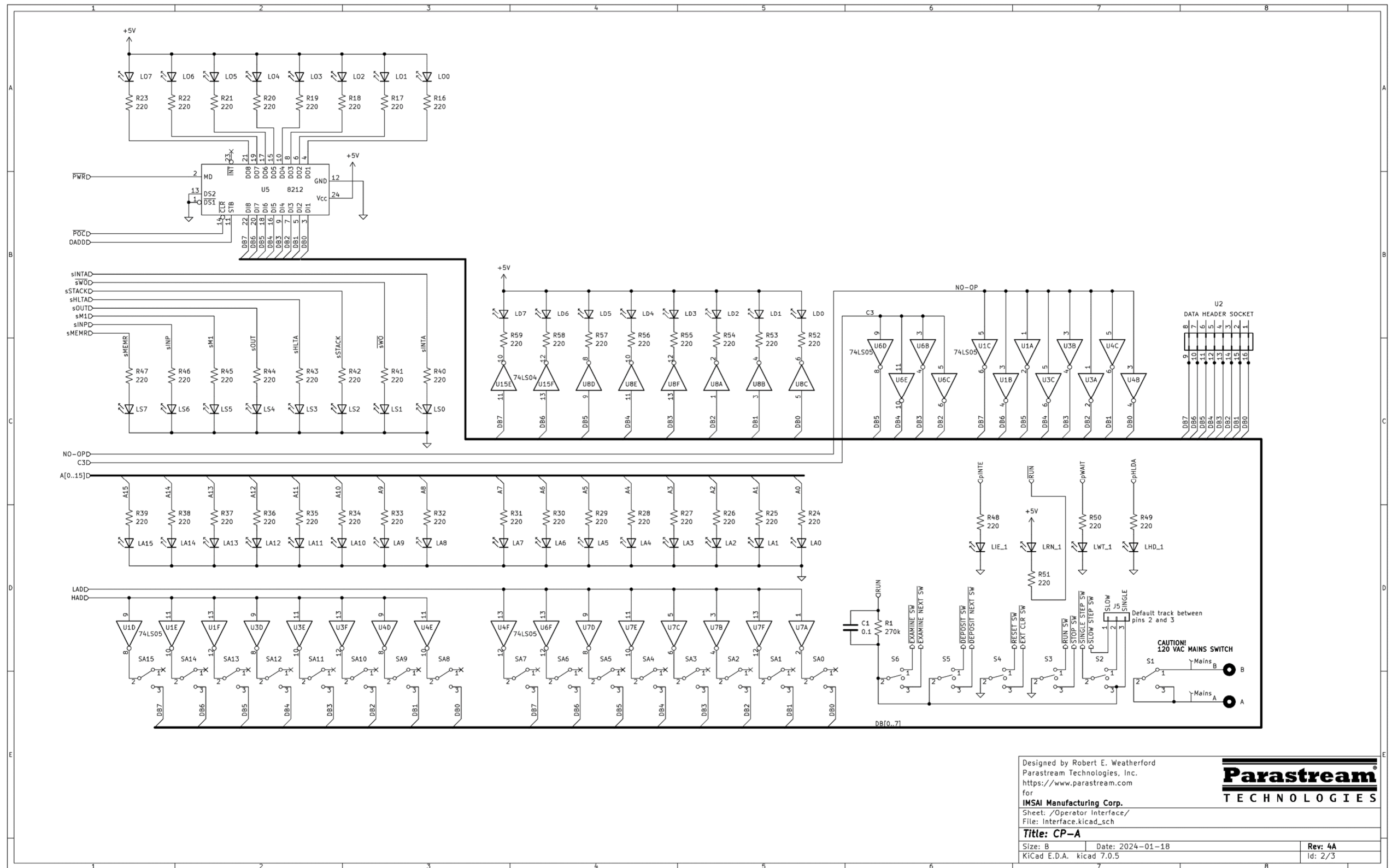


Figure 3. Schematic Diagram, Operator Interface

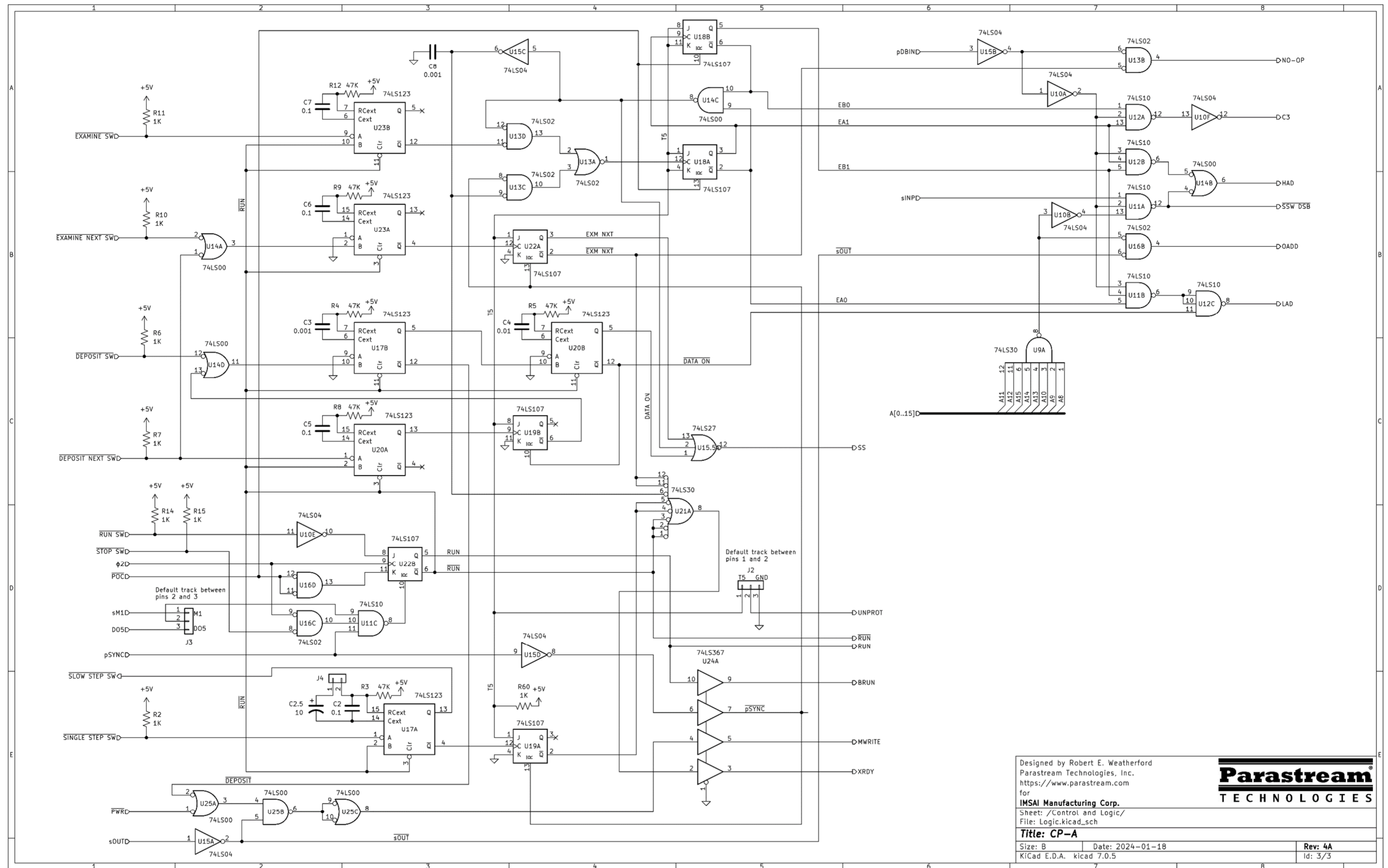


Figure 4. Schematic Diagram, Control and Logic

ASSEMBLY DIAGRAM

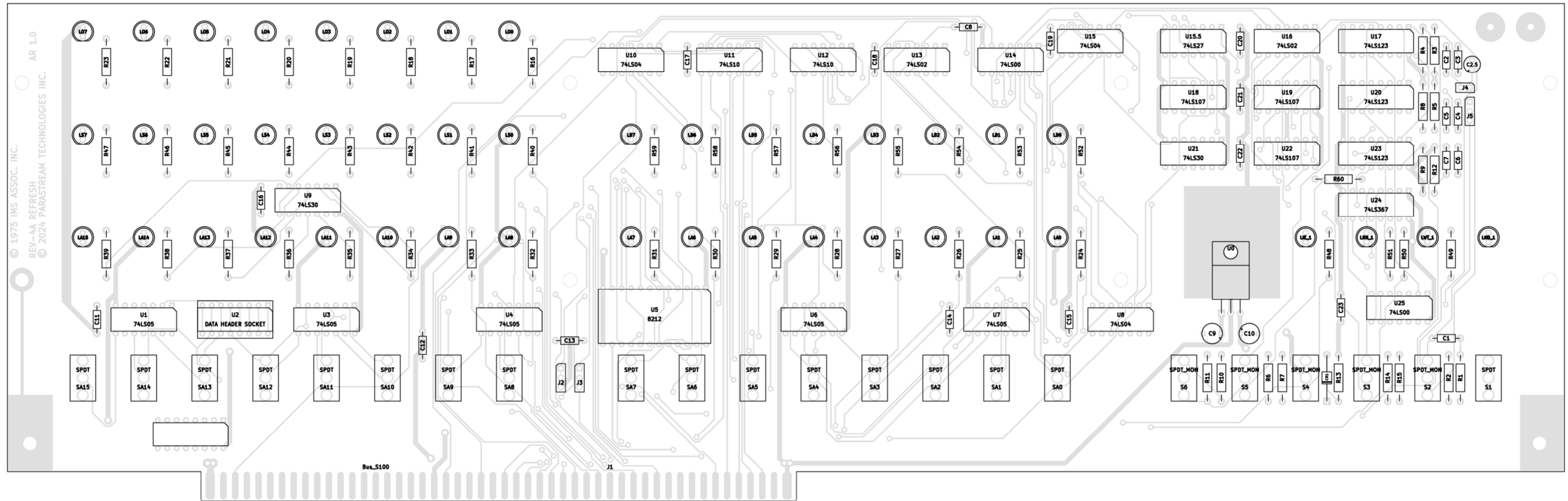


Figure 5. Assembly Diagram

REVISION HISTORY

Revision	Date	Initial	Description
0.0	1/17/2024	REW	Document currently under initial construction.