256K x 16 High Speed EDO DRAM

(04/1997)

Features

- Fast Access Time: 50ns/60ns
- Fast EDO Page Cycle Time: 20ns/25ns
- EDO Page Mode Operation
- Single +5V ±10% Power Supply
- Low Power Dissipation
- Individual Byte Control via Dual $\overline{\text{CAS}}$ Inputs
- Three Refresh Modes
  ($\overline{\text{RAS}}$-only, $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$, & Hidden Refresh)
- 512-Cycle Refresh in 8ms
  (9 rows and 9 columns)
- TTL Compatible
- 40-pin, 400-mil Plastic SOJ Package, or 40/44-Pin, 400-mil Plastic TSOP Package.

Ordering Information

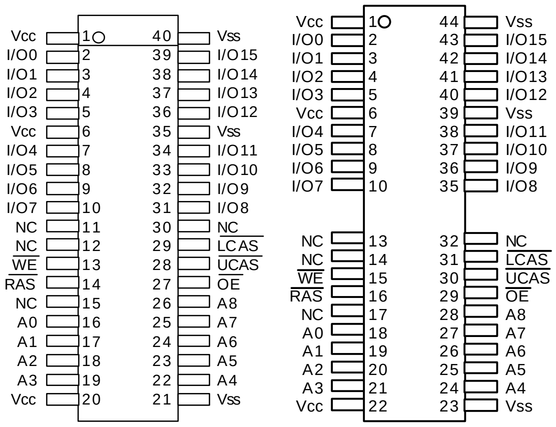
Part Number	Speed	Package
Em614163A-50	50ns	SOJ
EM614163TS-50	50ns	TSOP-II
Em614163A-60	60ns	SOJ
EM614163TS-60	60ns	TSOP-II

Key Specifications

Speed	tRAC	tCAC	tAA	tOEA	tRC	tPC
- 50	50ns	14ns	25ns	12ns	100ns	20ns
- 60	60ns	15ns	30ns	15ns	104ns	25ns

Pin Assignment (Top View)

40-Pin SOJ **40/44-Pin TSOP-II**



Pin Names

A0 - A8	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{UCAS}}$	Column Address Strobe (Upper Byte Control)
$\overline{\text{LCAS}}$	Column Address Strobe (Lower Byte Control)
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
I/O0 - I/O15	Data Input/Output
VCC	+5V Power Supply
VSS	Ground
NC	No Connection

Overview

The Em614163A is a high speed EDO (Extended Data Out) DRAM organized in 262,144 words by 16 bits. It supports EDO Page Mode and 16-bit data width for high data bandwidth applications. The EDO Page Mode is an accelerated access that provides a shorter page cycle and a faster data access time than the traditional Fast Page Mode.

Compared with Fast Page Mode DRAM, the EDO DRAM data output will be held valid after $\overline{\text{CAS}}$ goes HIGH, as long as $\overline{\text{RAS}}$ and $\overline{\text{OE}}$ are held LOW and $\overline{\text{WE}}$ is held HIGH. This feature allows $\overline{\text{CAS}}$ precharge time to occur without the output data going invalid. Therefore, the EDO $\overline{\text{CAS}}$ timing can be condensed to carry more data out in a given period.

The Em614163A fully utilizes the EDO Page Mode advantages. It allows 512 random access within a page with a fast cycle time as short as 20/25ns.

The Em614163A is ideally suitable for graphics frame buffers, CD-ROMs, disk drivers, set top boxes, and DSP applications.

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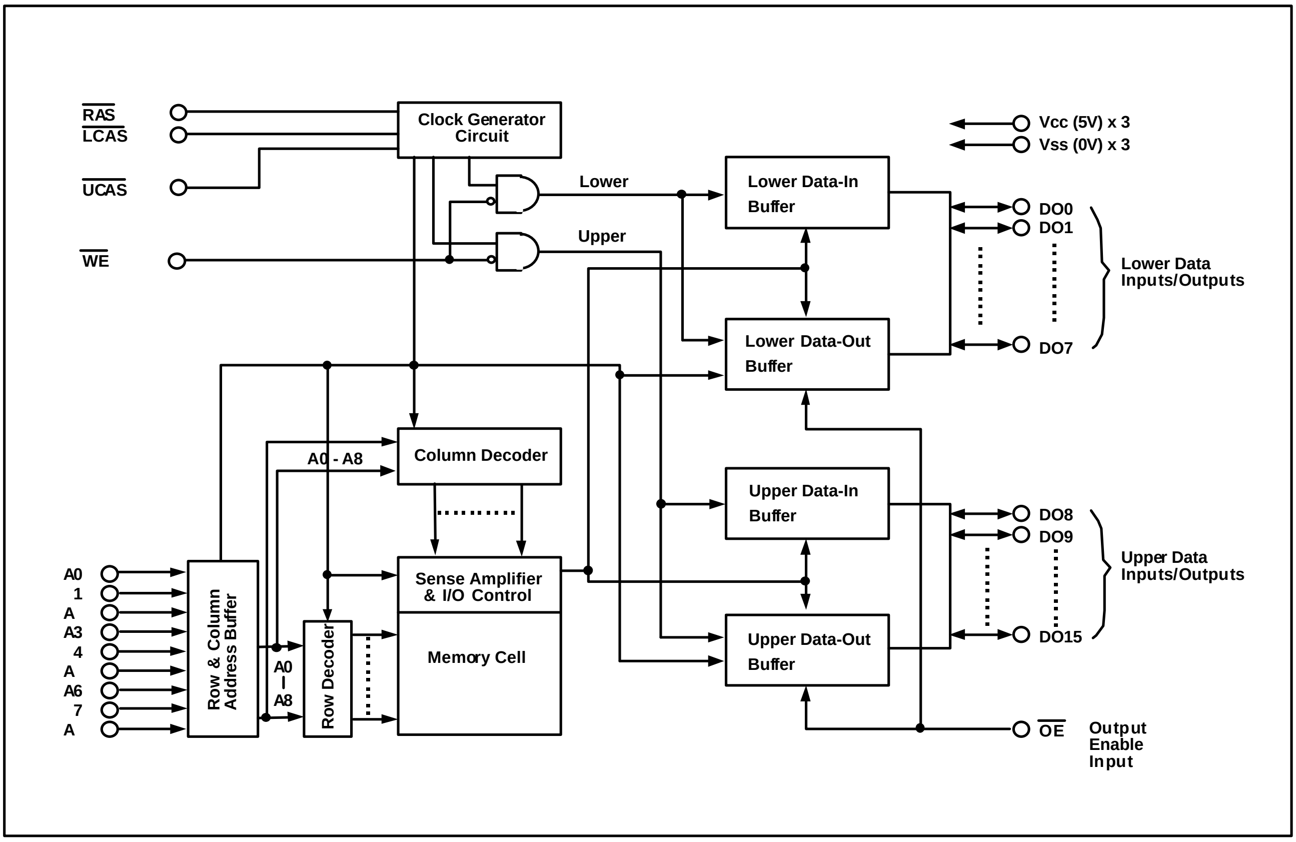
Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	- 0.5 to +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	- 0.5 to +7.0	V
Short circuit output current	I_{OUT}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{OPT}	0 to +70	°C
Storage temperature	T_{STG}	- 55 to +125	°C

Capacitance

(Ta = 25°C; Vcc = 5V±10%; f = 1MHz)

Parameter	Symbol	Typ	Max	Unit	Note
Input capacitance (A0 - A8)	C_{I1}	¡ Ð	5	pF	1
Input capacitance ($\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$)	C_{I2}	¡ Ð	7	pF	1
Output capacitance(I/O0 - I/O15)	$C_{I/O}$	¡ Ð	5	pF	1,2

Notes:

1. Capacitance measured with Boonton Meter or effective capacitance measuring methods.
2. $\overline{LCAS}$ = $\overline{UCAS}$ = V_{IH} to disable Dout.

Truth Table

Function		$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	Addresses		DQs	Notes
							t_R	t_C		
Standby		H	H→X	H→X	X	X	X	X	High-Z	
Read: Word		L	L	L	H	L	ROW	COL	Data-outt	
Read: Lower Byte		L	L	H	H	L	ROW	COL	Lower byte, data-out Upper byte, high-Z	
Read: Upper Byte		L	H	L	H	L	ROW	COL	Lower byte, high-Z Upper byte, data-out	
Write: Word (Early Write)		L	L	L	L	X	ROW	COL	Data-in	
Write: Lower Byte (Early)		L	L	H	L	X	ROW	COL	Lower byte, data-in Upper byte, high-Z	
Write: Upper Byte (Early)		L	H	L	L	X	ROW	COL	Lower byte, high-Z Upper byte, data-in	
Read Write		L	L	L	H→L	L→H	ROW	COL	Data-out, Data-in	1, 2
EDO-Page-Mode Read	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-out	2
EDO-Page-Mode Write	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-in	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-in	1
EDO-Page-Mode Read-Write	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-out, Data-in	1, 2
	2nd Cycle	L	H→L	H→L	H→L	L→H	n/a	COL	Data-out, Data-in	1, 2
Hidden Refresh	Read	L→H→L	L	L	H	L	ROW	COL	Data-out	2
	Write	L→H→L	L	L	L	X	ROW	COL	Data-in	1, 3
RAS# only refresh		L	H	H	X	X	ROW	n/a	High-Z	
CBR Refresh		H→L	L	L	X	X	X	X	High-Z	4

Note:

1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{LCAS}$ or $\overline{UCAS}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{LCAS}$ or $\overline{UCAS}$ active).
3. EARLY WRITE only.
4. At least one of the two $\overline{CAS}$ signals must be active ($\overline{LCAS}$ or $\overline{UCAS}$).

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V_{SS}	0	0	0	V	2
	V_{CC}	4.5	5.0	5.5	V	1, 2
Input high voltage	V_{IH}	2.4	¡ Ð	V_{CC} + 0.3	V	1
Input low voltage	V_{IL}	- 0.5	¡ Ð	0.8	V	1, 3

Notes:

1. All voltage referenced to V_{SS}.
2. The supply voltage with all V_{CC} pins must be the same level.
   The supply voltage with all V_{SS} pins must be the same level.
3. V_{IL} Min. = - 1.2V for pulse width ¡ 30ns.

DC Characteristics

T_A = 0 to +70°C; Vcc = +5V ± 10%, Vss = 0V

Parameter	Symbol	Test Conditions	Em614163A				Unit	Notes
			- 50		- 60			
			Min	Max	Min	Max		
Operating current	ICC1	$\overline{RAS}$ cycling $\overline{LCAS}$, $\overline{UCAS}$ cycling t_{RC} = min.	-	180	-	150	mA	1, 2
Standby current	ICC2	$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$ = VIH Dout = High-Z	-	2	-	2	mA	
		$\overline{RAS}$, $\overline{LCAS}$, $\overline{UCAS}$, $\overline{OE}$ = VCC - 0.2V Dout = High-Z	-	1	-	1	mA	
$\overline{RAS}$-only refresh current	ICC3	$\overline{RAS}$ cycling, $\overline{CAS}$ = VIH t_{RC} = min.	-	180	-	150	mA	2
Standby current	ICC5	RAS = VIH $\overline{LCAS}$, $\overline{UCAS}$ = VIL Dout = enable	-	5	-	5	mA	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	ICC6	t_{RC} = min. $\overline{RAS}$, $\overline{CAS}$ cycling	-	180	-	150	mA	
Fast page mode current	ICC7	tPC = min.		180		150	mA	1, 3
Input leakage current	ILI	0V ¡ Õ Vin ¡ Õ VCC	- 10	10	- 10	10	µA	
Output leakage current	ILO	0V ¡ Õ Vout ¡ Õ VCC Dout = Disable	- 10	10	- 10	10	µA	
Output high voltage	VOH	IOH = - 2.5 mA	2.4		2.4		V	
Output low voltage	VOL	IOL = + 2.1 mA		0.4		0.4	V	

Notes:

1. I_{CC} depends on output load condition when the device is selected. I_{CC}-max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.
3. Address can be changed once or less while $\overline{LCAS}$ and $\overline{UCAS}$ = V_{IH}.
4. All the V_{CC} pins shall be supplied with the same voltage. And all the V_{SS} pins shall be supplied with the same voltage.

AC Characteristics (2, 3, 4, 5)

(Ta = 0 to +70°C; Vcc = 5V±10%, Vss = 0V)

Test Conditions

- Input rise and fall times: 5ns
- AC test condition, input pulse levels 0V to 3V
- Output load: 2 TTL loads and 100pF
- Output timing reference levels: V_{OH} = 2.0V
  V_{OL} = 0.8V

Read, Write, Read-Modify-Write and Refresh Cycles

(Common Parameters)

Parameter	Symbol	Em614163A				Unit	Notes
		- 50		- 60			
		Min	Max	Min	Max		
Random read or write cycle time	t_{RC}	100	-	104	-	ns	1
$\overline{\text{RAS}}$ precharge time	t_{RP}	40	-	40	-	ns	
$\overline{\text{RAS}}$ pulse width	t_{RAS}	50	100,000	60	100,000	ns	6
$\overline{\text{U/LCAS}}$ pulse width	t_{CAS}	8	100,000	10	100,000	ns	7
Row address setup time	t_{ASR}	0	-	0	-	ns	
Row address hold time	t_{RAH}	8	-	10	-	ns	
Column address setup time	t_{ASC}	0	-	0	-	ns	8
Column address hold time	t_{CAH}	8	-	10	-	ns	8
$\overline{\text{RAS}}$ to $\overline{\text{U/LCAS}}$ delay time	t_{RCD}	14	36	14	45	ns	9
$\overline{\text{RAS}}$ to column address delay time	t_{RAD}	11	25	12	30	ns	10
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	24	-	30	-	ns	
$\overline{\text{RAS}}$ hold time	t_{RSH}	8	-	10	-	ns	
$\overline{\text{U/LCAS}}$ hold time	t_{CSH}	50	-	55	-	ns	
Column address hold time from $\overline{\text{RAS}}$	t_{AR}	40	-	50	-	ns	
Write command timefrom $\overline{\text{RAS}}$	t_{WCR}	40	-	50	-	ns	
Data-in hold time from $\overline{\text{RAS}}$	t_{DHR}	40	-	50	-	ns	
$\overline{\text{U/LCAS}}$ to $\overline{\text{RAS}}$ precharge time	t_{CRP}	5	-	5	-	ns	11
$\overline{\text{OE}}$ to Din delay time	t_{OED}	8	-	10	-	ns	
Transition time (rise and fall)	t_{T}	1	50	1	50	ns	12
Refresh period	t_{REF}	-	8	-	8	ms	
$\overline{\text{CAS}}$ to output in Low-Z	t_{CLZ}	0	-	0	-	ns	

Read Cycle

Parameter	Symbol	Em614163A				Unit	Notes
		- 50		- 60			
		Min	Max	Min	Max		
Access time from $\overline{\text{RAS}}$	t_{RAC}	-	50	-	60	ns	13
Access time from $\overline{\text{U/LCAS}}$	t_{CAC}	-	14	-	15	ns	14, 15, 16
Access time from column address	t_{AA}	-	25	-	30	ns	15, 17
Access time from $\overline{\text{OE}}$	t_{OEA}	-	12	-	15	ns	
Read command setup time	t_{RCS}	0	-	0	-	ns	8
Read command hold time to $\overline{\text{U/LCAS}}$	t_{RCH}	0	-	0	-	ns	11, 18
Read command hold time to $\overline{\text{RAS}}$	t_{RRH}	0	-	0	-	ns	18
Output buffer turn-off time	t_{OFF}	0	8	0	10	ns	19
Output buffer turn-off $\overline{\text{OE}}$	t_{OEZ}	0	8	0	10	ns	19
Write Cycle							
Write command setup time	t_{WCS}	0	-	0	-	ns	8, 20
Write command hold time	t_{WCH}	7	-	10	-	ns	8
Write command pulse width	t_{WP}	7	-	10	-	ns	
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	12	-	12	-	ns	
Write command to $\overline{\text{U/LCAS}}$ lead time	t_{CWL}	8	-	10	-	ns	21
Data-in setup time	t_{DS}	0	-	0	-	ns	22
Data-in hold time	t_{DH}	8	-	10	-	ns	22
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$	t_{OEH}	8	-	10	-	ns	

Read-Modify-Write Cycle

Parameter	Symbol	Em614163A				Unit	Notes
		- 50		- 60			
		Min	Max	Min	Max		
Read-modify-write cycle time	t_{RWC}	126	-	140	-	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ delay time	t_{RWD}	68	-	77	-	ns	20
$\overline{\text{U/LCAS}}$ to $\overline{\text{WE}}$ delay time	t_{CWD}	32	-	32	-	ns	20
Column address to $\overline{\text{WE}}$ delay time	t_{AWD}	43	-	47	-	ns	20
Refresh Cycle							
$\overline{\text{U/LCAS}}$ setup time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle)	t_{CSR}	5	-	5	-	ns	8
$\overline{\text{U/LCAS}}$ hold time ($\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh cycle)	t_{CHR}	10	-	10	-	ns	11
$\overline{\text{RAS}}$ precharge to $\overline{\text{U/LCAS}}$ hold time	t_{RPC}	5	-	5	-	ns	8
$\overline{\text{U/LCAS}}$ precharge time in normal mode	t_{CPN}	10	-	10	-	ns	23

EDO Page Mode Cycle

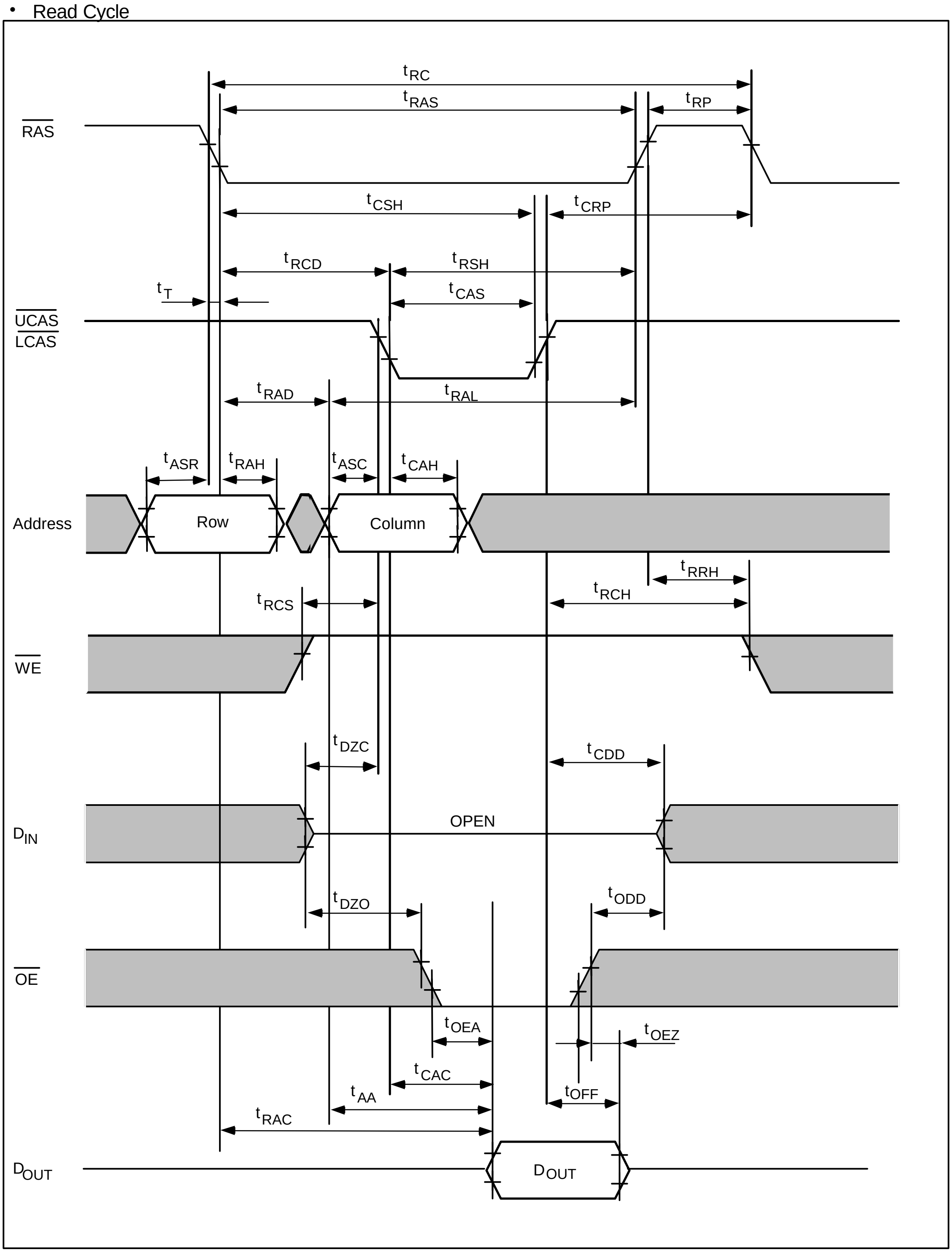
Parameter	Symbol	Em614163A				Unit	Notes
		- 50		- 60			
		Min	Max	Min	Max		
EDO page mode cycle time	t_{PC}	20	-	25	-	ns	25
EDO page mode $\overline{\text{U/LCAS}}$ precharge time	t_{CP}	8	-	10	-	ns	23
EDO page mode $\overline{\text{RAS}}$ pulse width	t_{RASP}	-	100000	-	100000	ns	24
Access time from $\overline{\text{U/LCAS}}$ precharge	t_{CPA}	-	30	-	35	ns	11, 15
$\overline{\text{RAS}}$ hold time from $\overline{\text{U/LCAS}}$ precharge	t_{CPRH}	30	-	35	-	ns	
EDO page mode read-modify-write cycle $\overline{\text{U/LCAS}}$ precharge to $\overline{\text{WE}}$ delay time	t_{CPW}	48	-	55	-	ns	11
EDO page mode read-modify-write cycle time	t_{PRWC}	64	-	66	-	ns	
$\overline{\text{OE}}$ low to $\overline{\text{CAS}}$ high setup time	t_{OES}	5	-	5	-	ns	
$\overline{\text{OE}}$ high hold time from $\overline{\text{CAS}}$ high	t_{OEHC}	8	-	10	-	ns	
$\overline{\text{OE}}$ high pulse width	t_{OEP}	7	-	10	-	ns	
$\overline{\text{OE}}$ setup prior to $\overline{\text{RAS}}$ during hidden refresh cycle	t_{ORD}	0	-	0	-	ns	
Data output hold after $\overline{\text{CAS}}$ low	t_{COH}	5	-	5	-	ns	
Output disable delay from $\overline{\text{WE}}$	t_{WHZ}	0	13	0	13	ns	
$\overline{\text{WE}}$ pulse width for output disable when $\overline{\text{CAS}}$ high	t_{WPZ}	7	-	7	-	ns	
Counter Test Cycle							
$\overline{\text{U/LCAS}}$ precharge time in counter test cycle	t_{CPT}	30	-	30	-	ns	23

Notes:

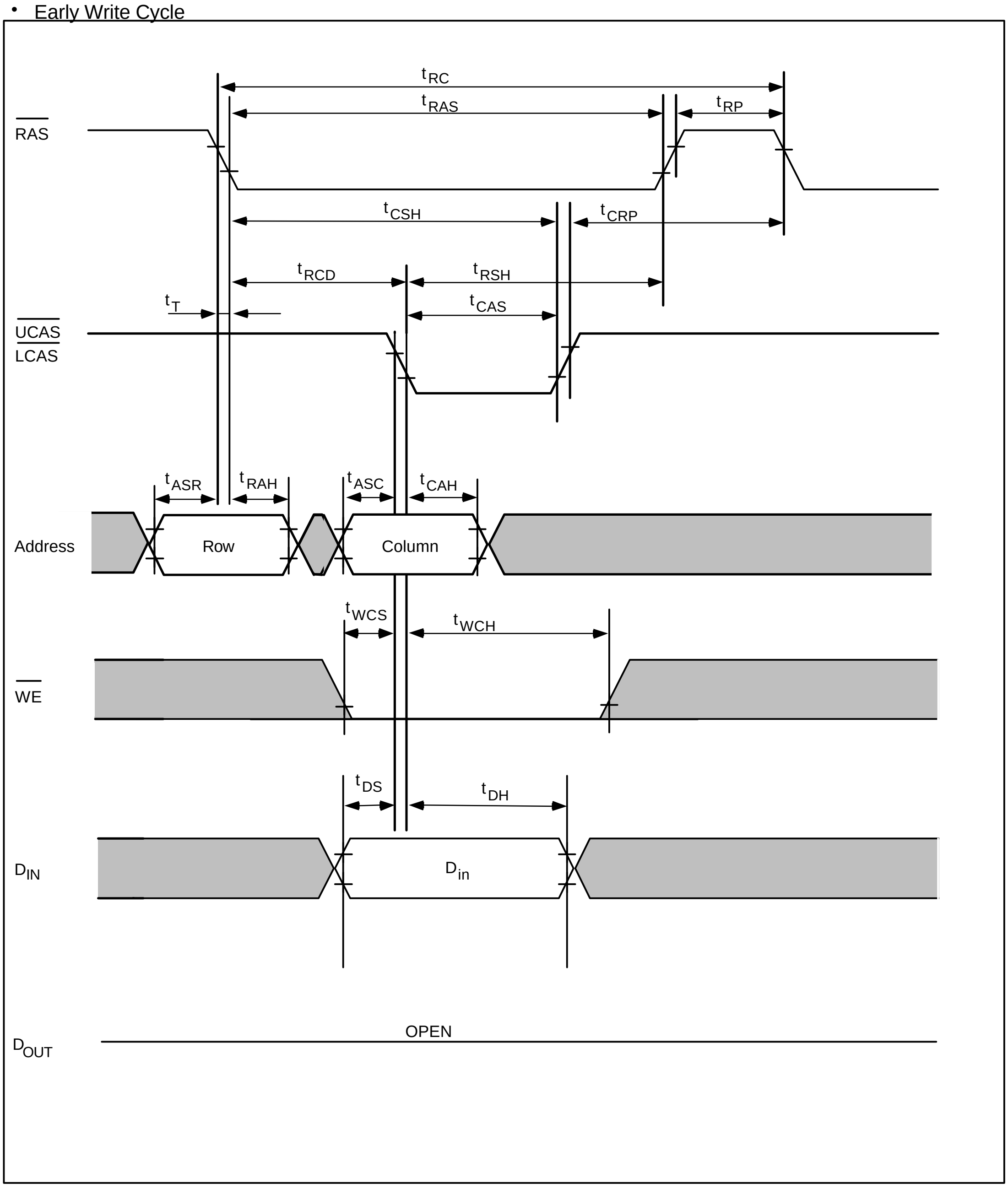
1. Assume t_T = 5ns.
2. An initial pause of 100 us is required after power up followed by a minimum of eight initialization cycles ($\overline{RAS}$-only refresh cycle or $\overline{CAS}$-beofre-$\overline{RAS}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles are required.
3. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device.
4. When both $\overline{LCAS}$ and $\overline{UCAS}$ go low at the same time, all 16-bits data are written into the device. $\overline{LCAS}$ and $\overline{UCAS}$ cannot be straggered within the same write/read cycles.
5. All the V_{CC} and all the V_{SS} pins shall be supplied with the same voltages.
6. t_{RAS}(min) = t_{RWD}(min) + t_{RWL}(min) + t_T in read-modify-write cycle.
7. t_{CAS}(min) = t_{CWD}(min) + t_{CWL}(min) + t_T in read-modify-write cycle.
8. t_{ASC}, t_{CAH}, t_{RCS}, t_{CSR}, t_{WCS}, t_{WCH}, and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
9. Operation with the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.
10. Operation with the t_{RAD}(max) limit insures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled exclusively by t_{AA}.
11. t_{CRP}, t_{CHR}, t_{RCH}, t_{CPA} and t_{CPW} are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
12. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
13. Assumes that $t_{RCD} \le t_{RCD}$(max) and $t_{RAD} \le t_{RAD}$(max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
14. Assumes that $t_{RCD} \ge t_{RCD}$(max) and $t_{RAD} \ge t_{RAD}$(max).
15. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
16. t_{CAC} is guaranteed for one TTL and 50pF load.
17. Assumes that $t_{RCD} \le t_{RCD}$(max) and $t_{RAD} \le t_{RAD}$(max).
18. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
19. t_{OFF}(max) and $t_{OEZ(}$max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. The t_{OFF} is determined by the later rising edge of $\overline{RAS}$ or $\overline{CAS}$.
20. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \ge t_{WCS}$(min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \ge t_{RWD}$(min), $t_{CWD} \ge t_{CWD}$(min), $t_{AWD} \ge t_{AWD}$(min) and $t_{CPW} \ge t_{CPW}$(min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
21. t_{CWL} shall be satisfied by both $\overline{UCAS}$, $\overline{LCAS}$.
22. These parameters are referenced to $\overline{UCAS}$ or $\overline{LCAS}$ leading edge in an early write cycle and to $\overline{WE}$ edge in a delayed write or a read-modify-write cycle.
23. t_{CPN}, t_{CP} and t_{CPT} are determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
24. t_{RASP} defines $\overline{RAS}$ pulse width in fast page mode cycles.
25. Assume t_T = 2ns.

Timing Waveforms

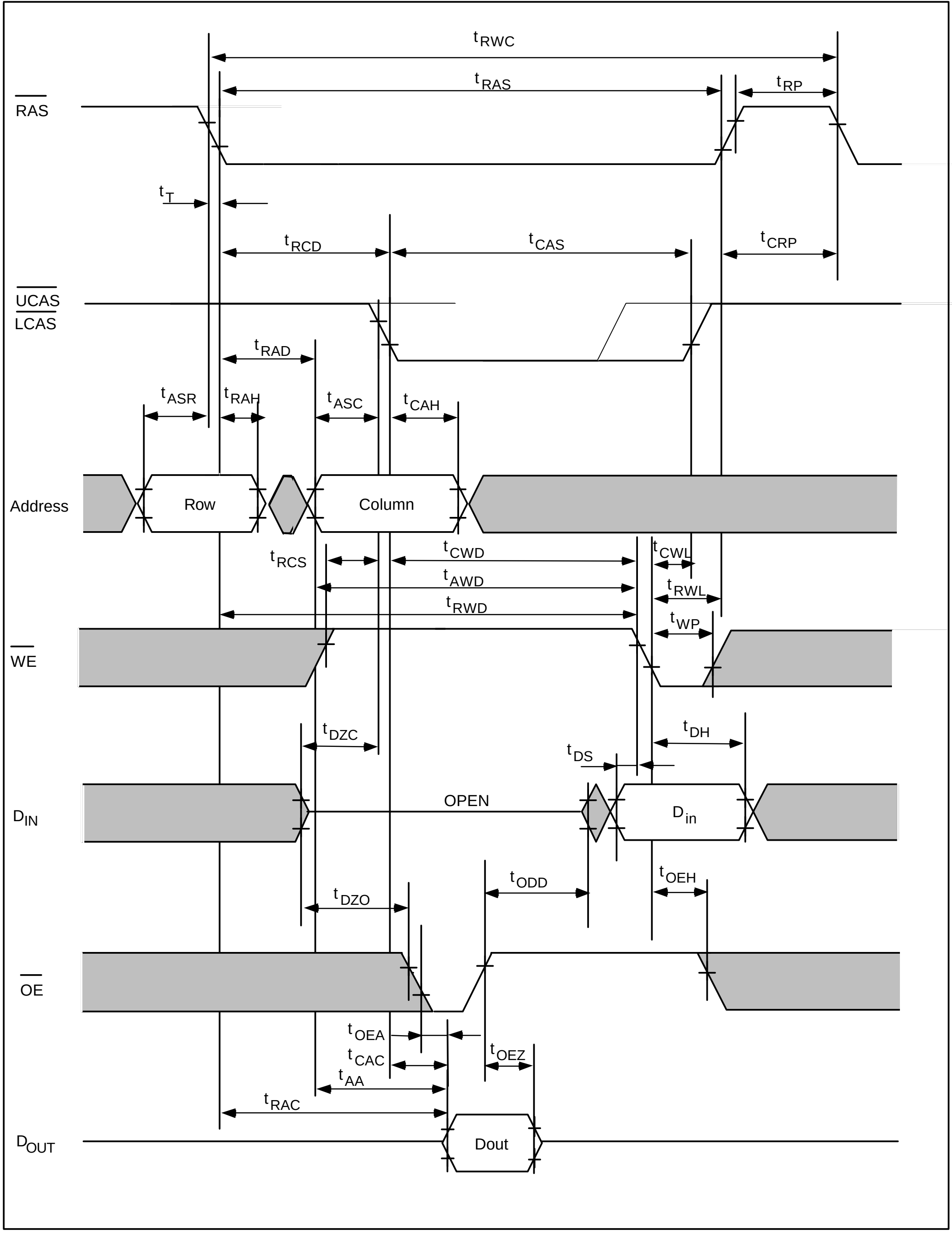
- Read Cycle



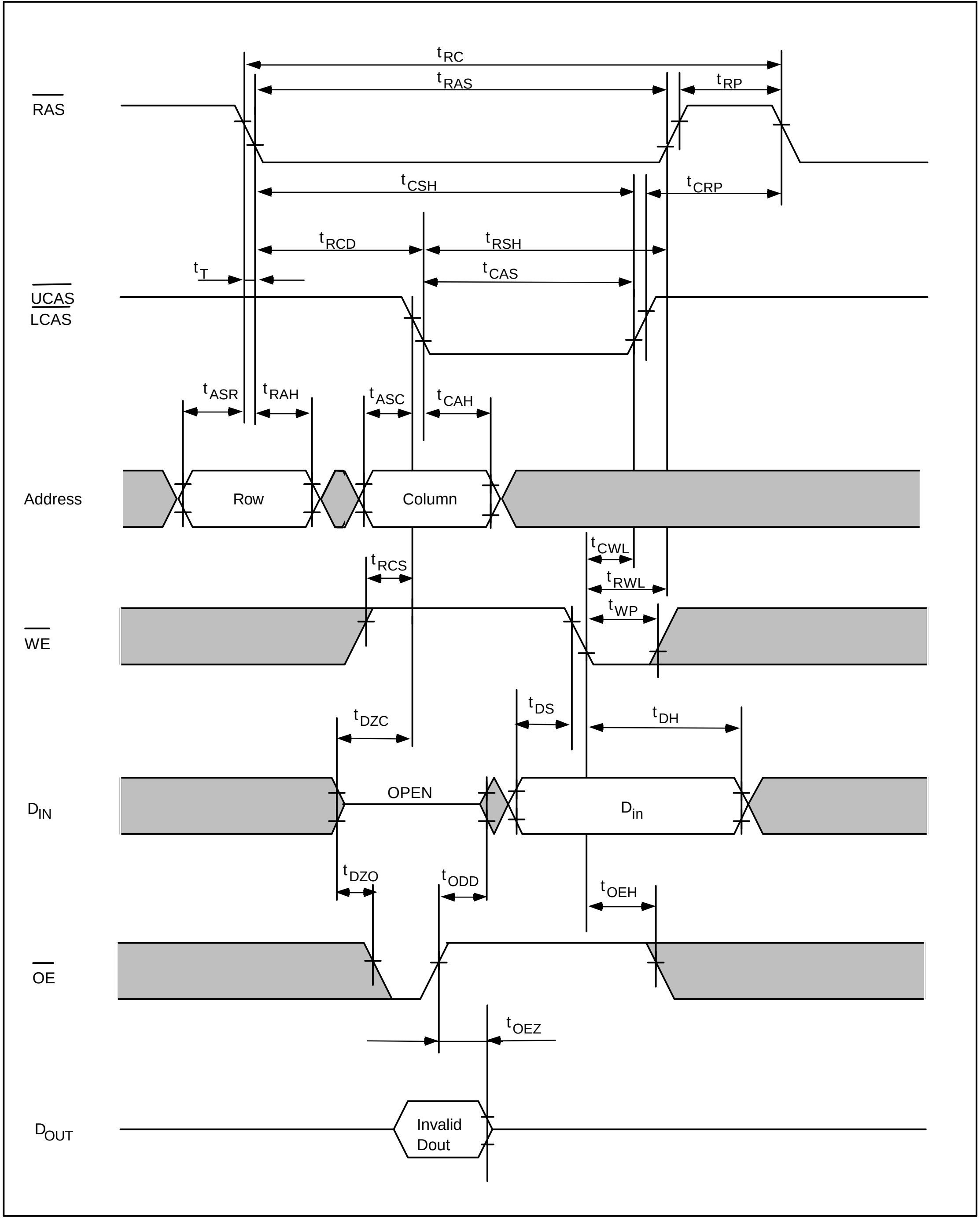
- Early Write Cycle



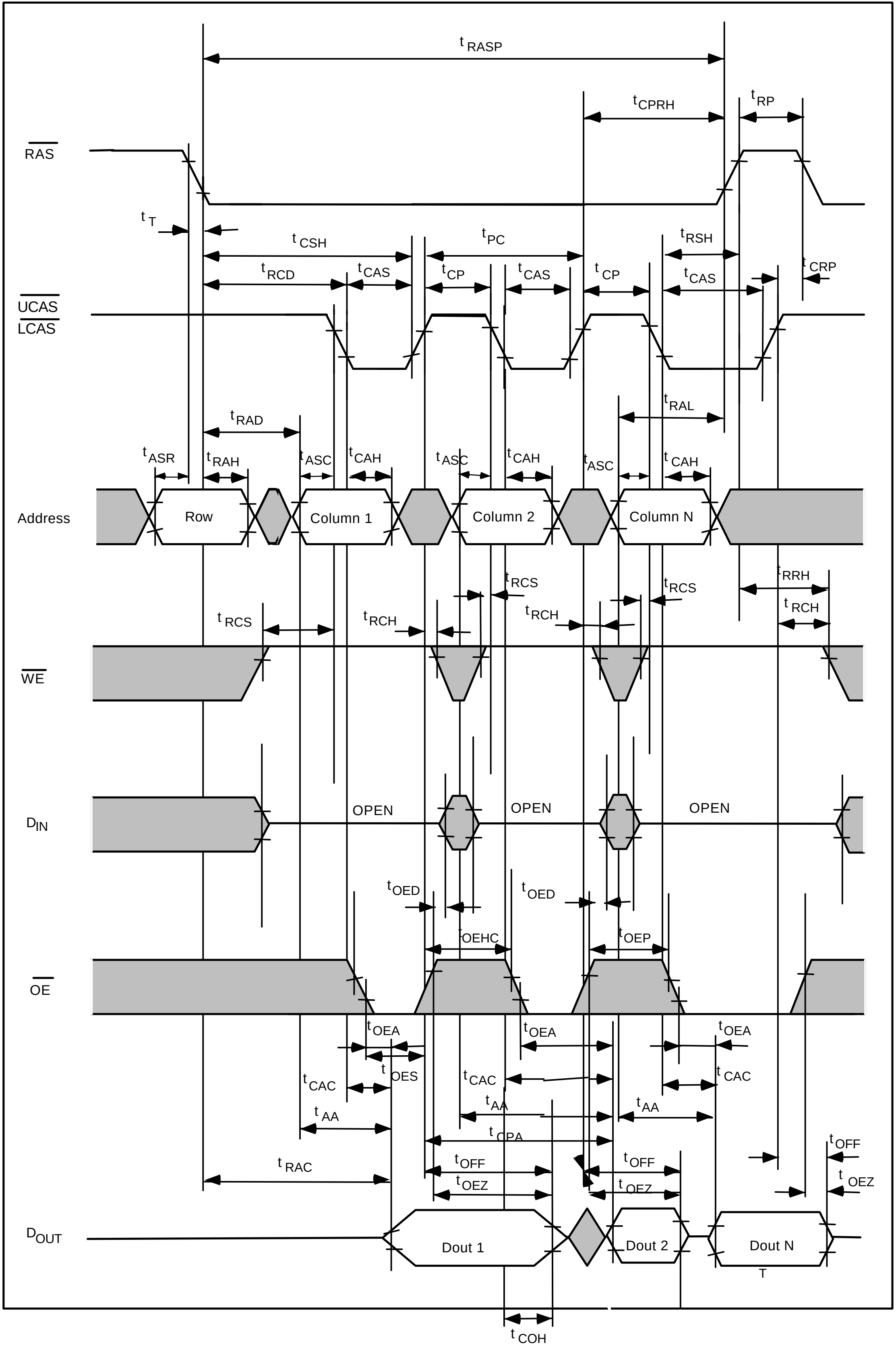
- Read-Modify-Write Cycle



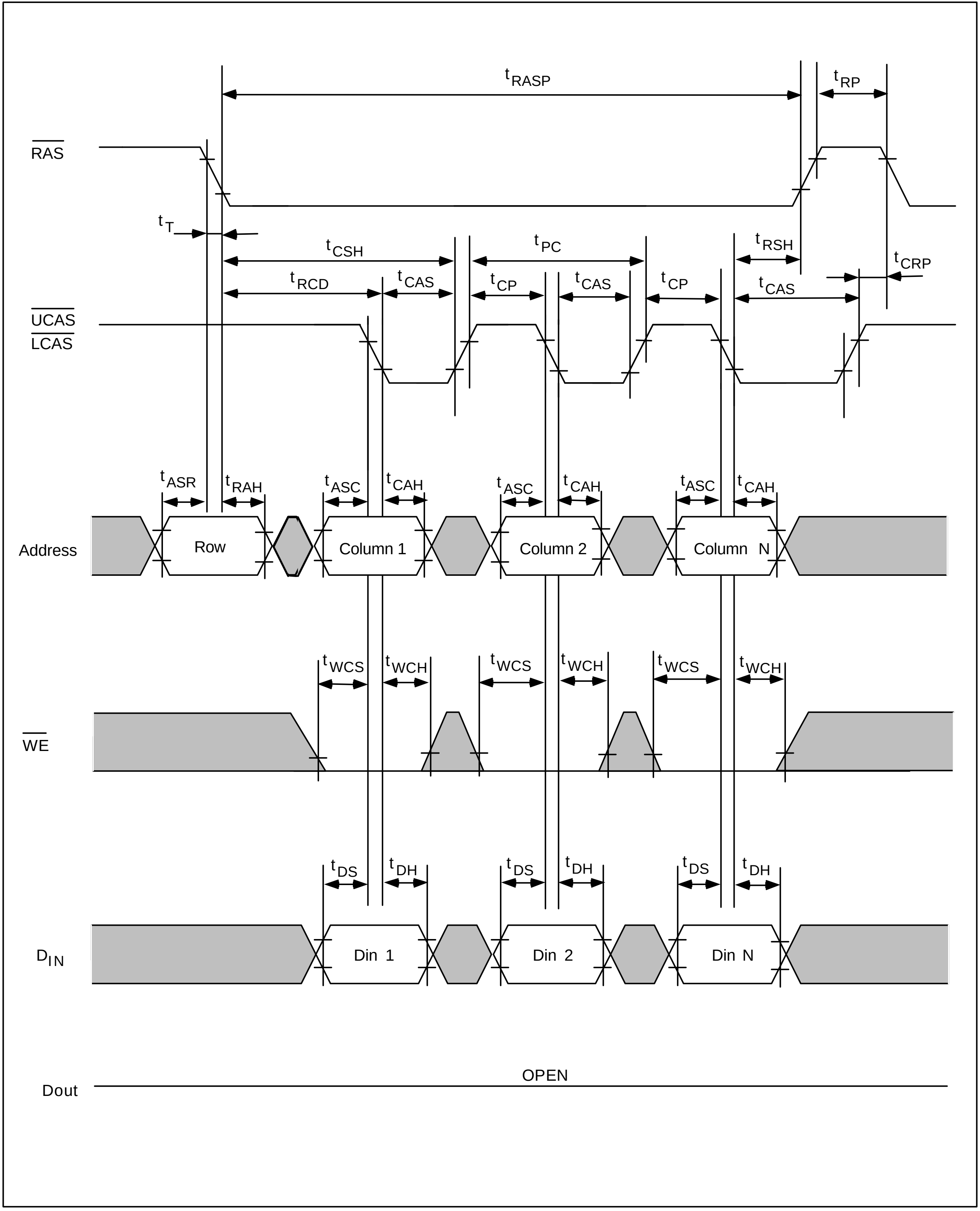
- Delayed Write Cycle



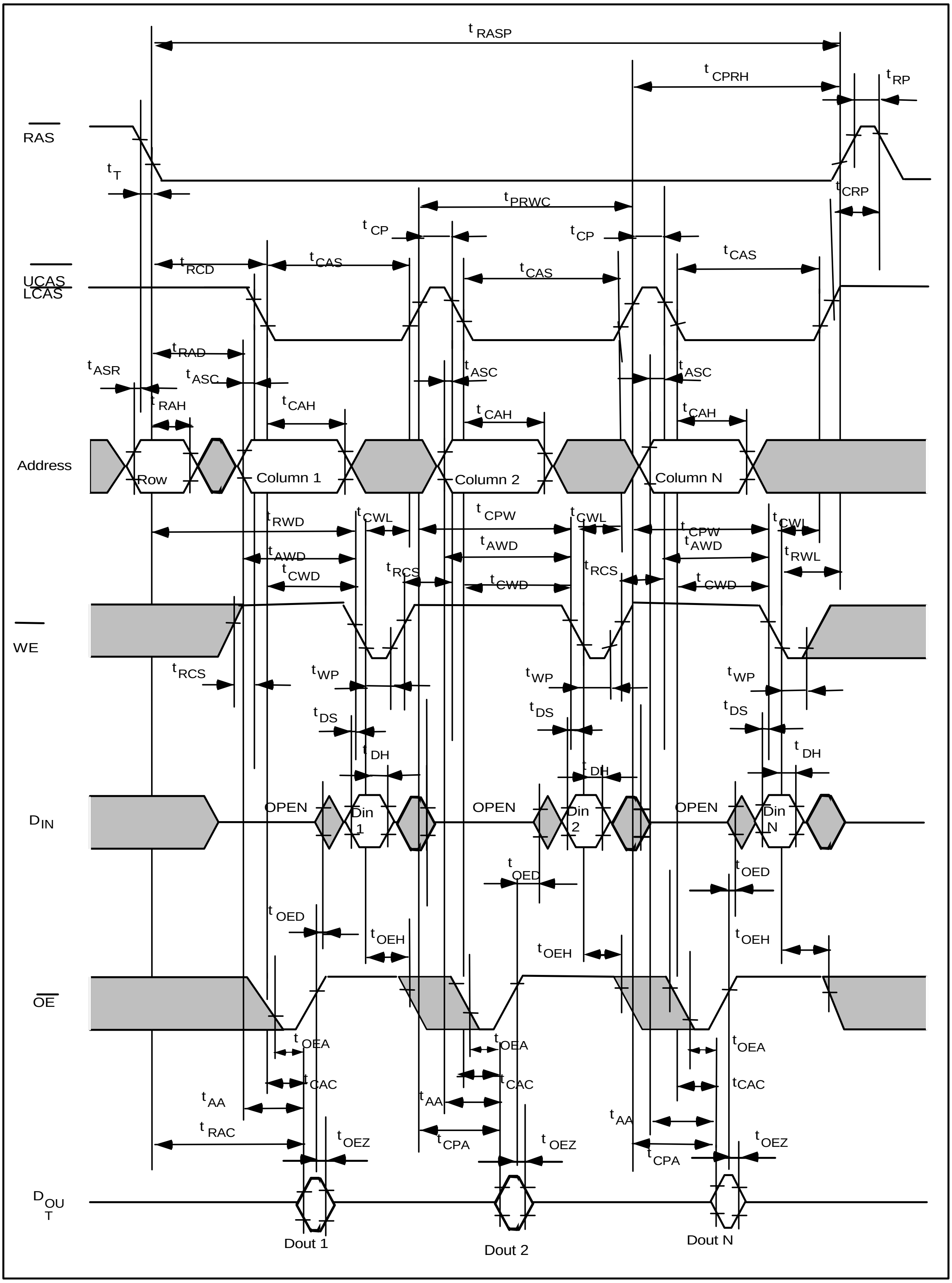
- EDO Page Mode Read Cycle



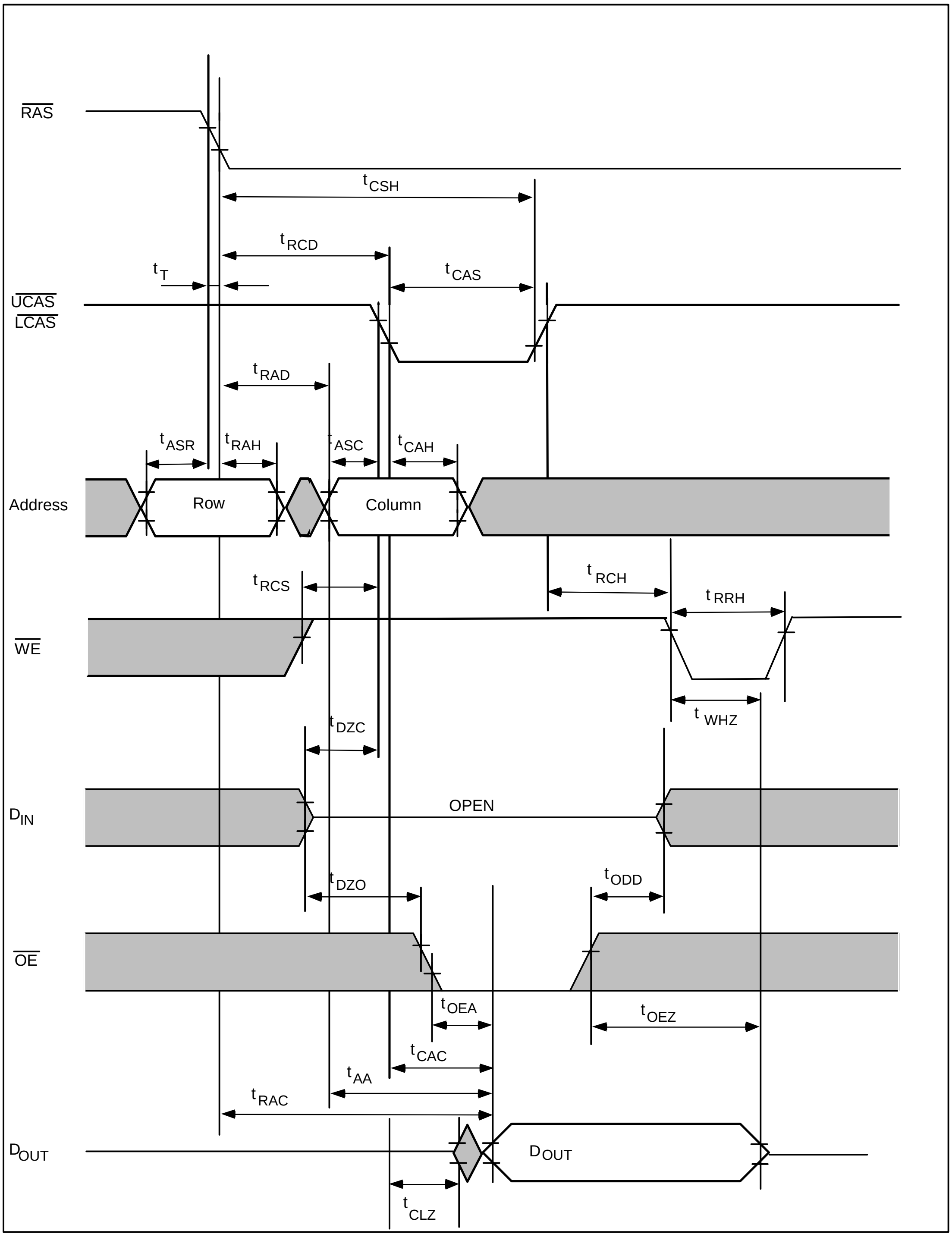
- EDO Page Mode Early Write Cycle



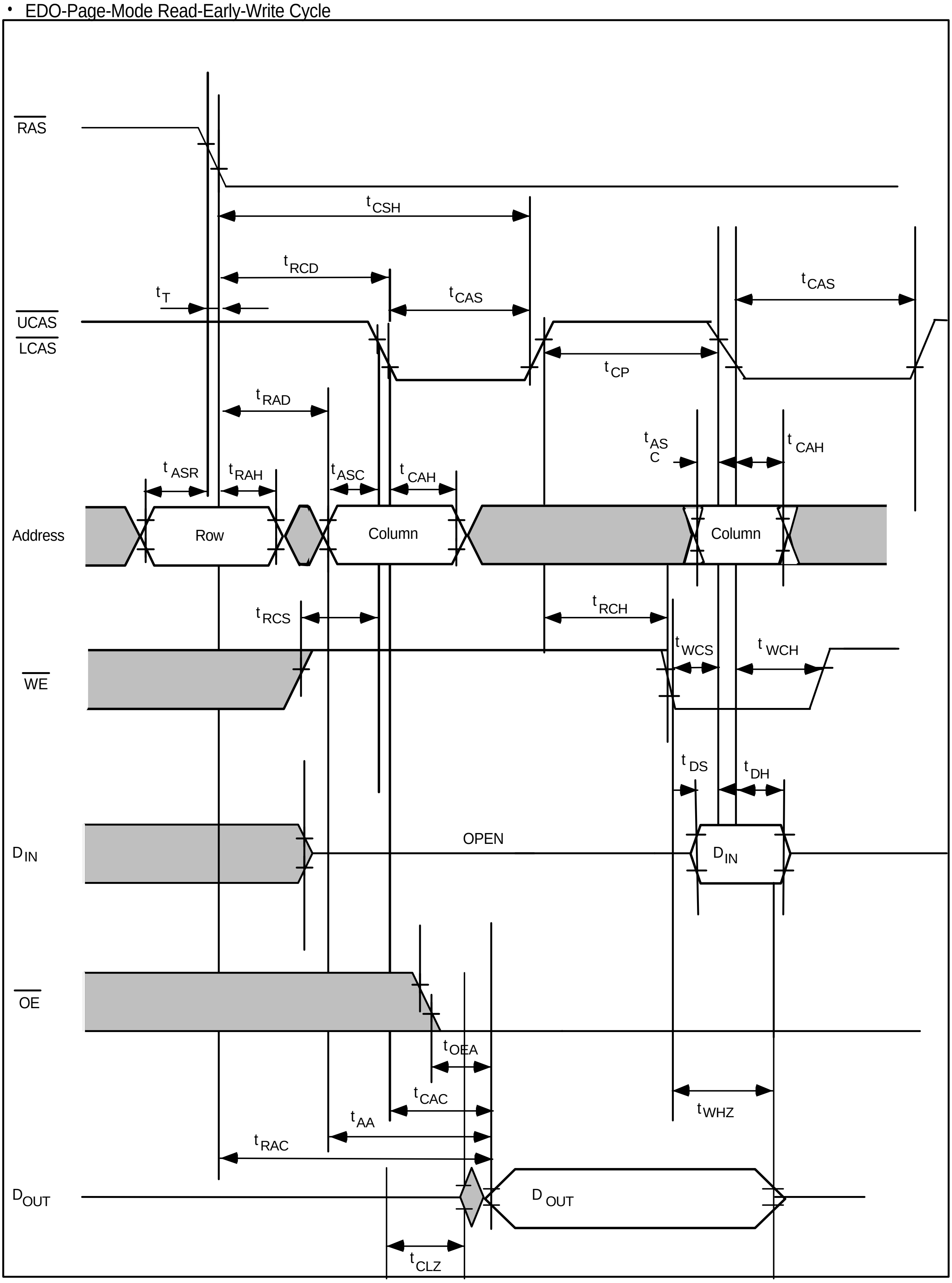
EDO Page Mode Read-Modify-Write Cycle



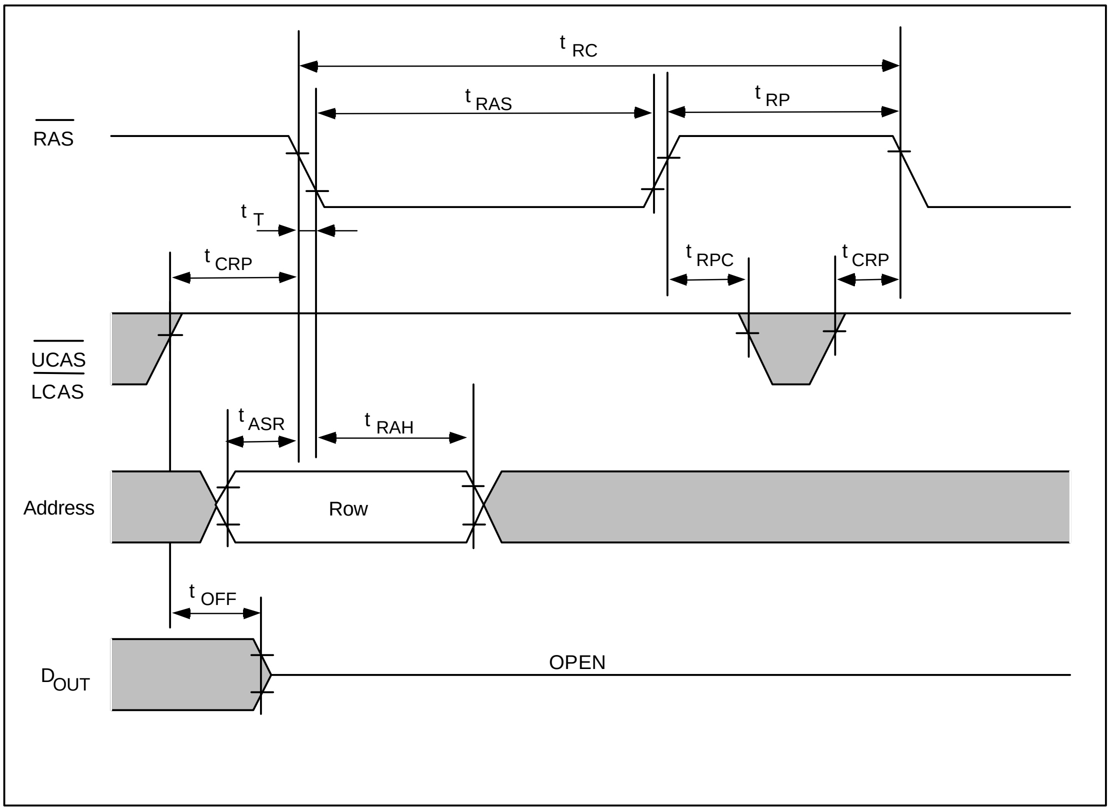
Read Cycle with $\overline{WE}$ Controlled Disable



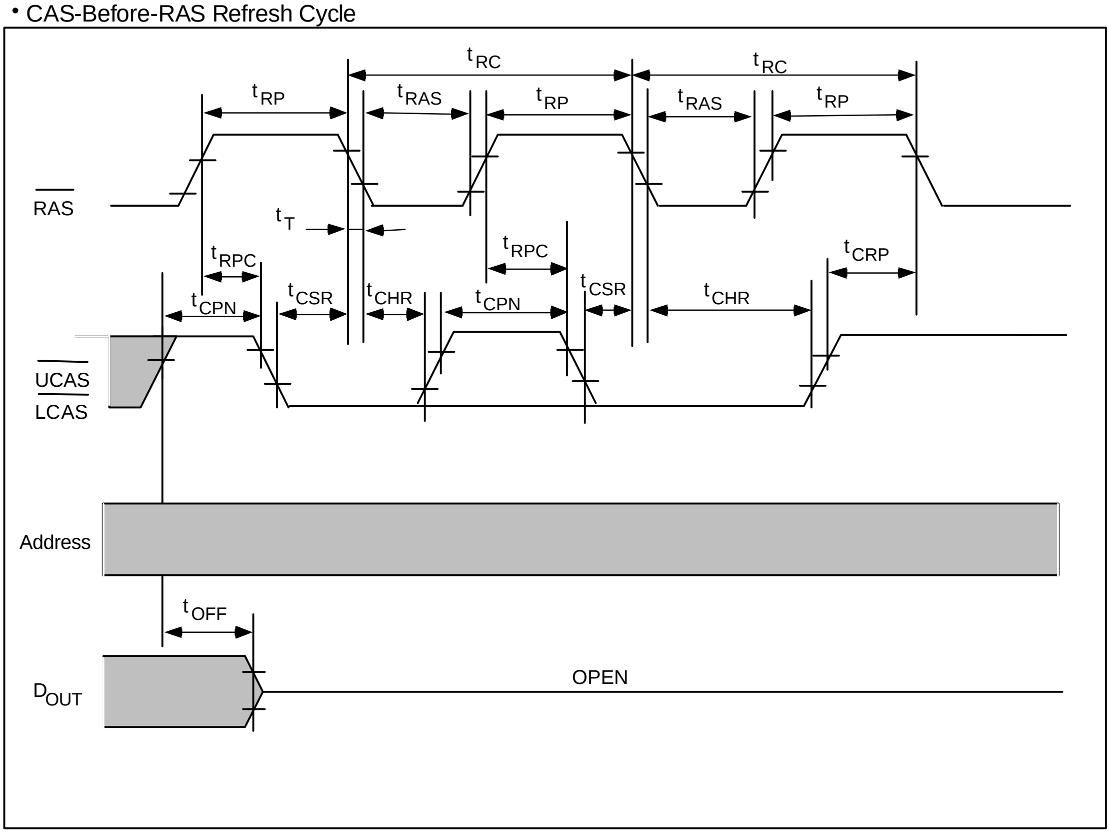
- EDO-Page-Mode Read-Early-Write Cycle



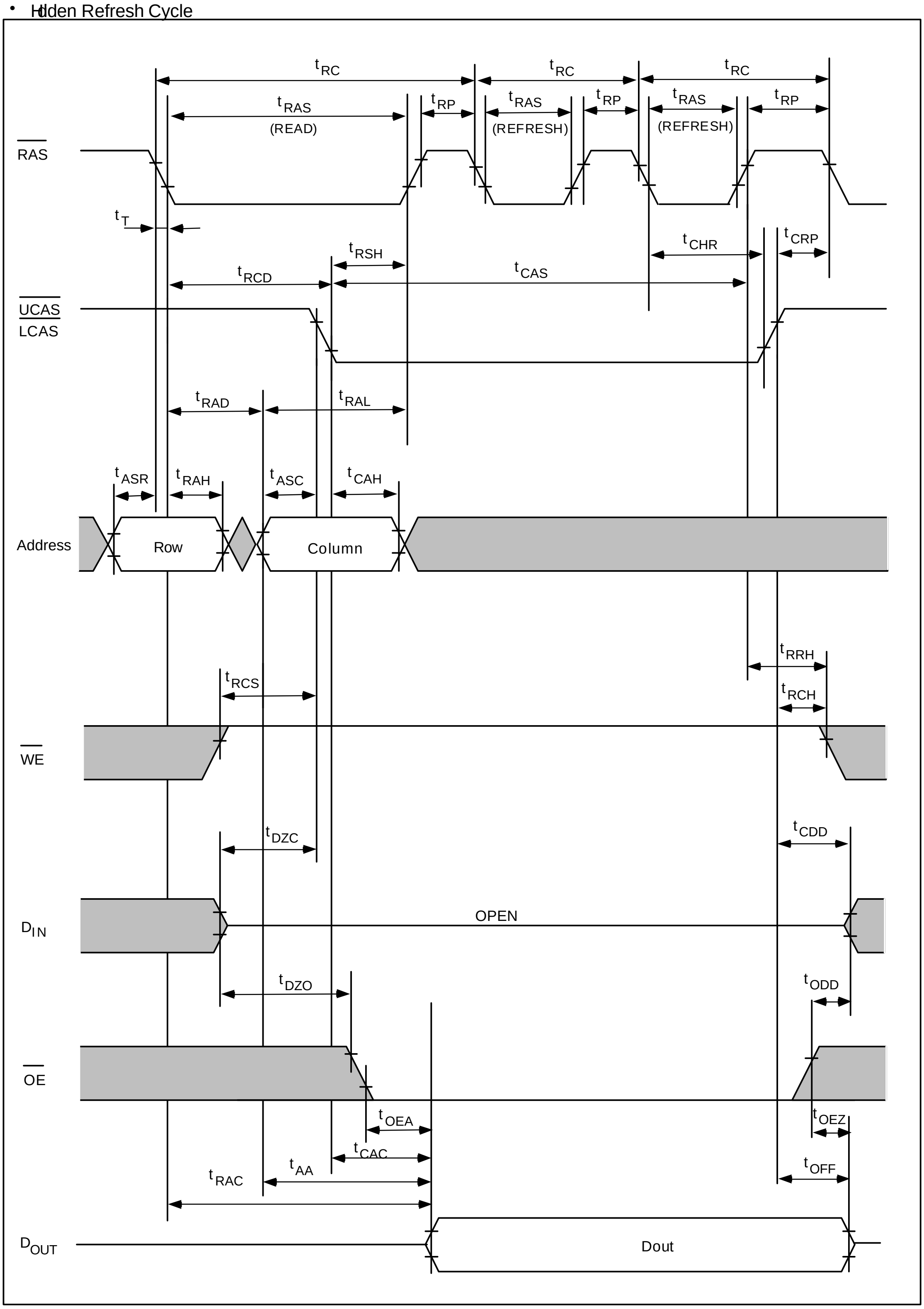
- RAS-Only Refresh Cycle



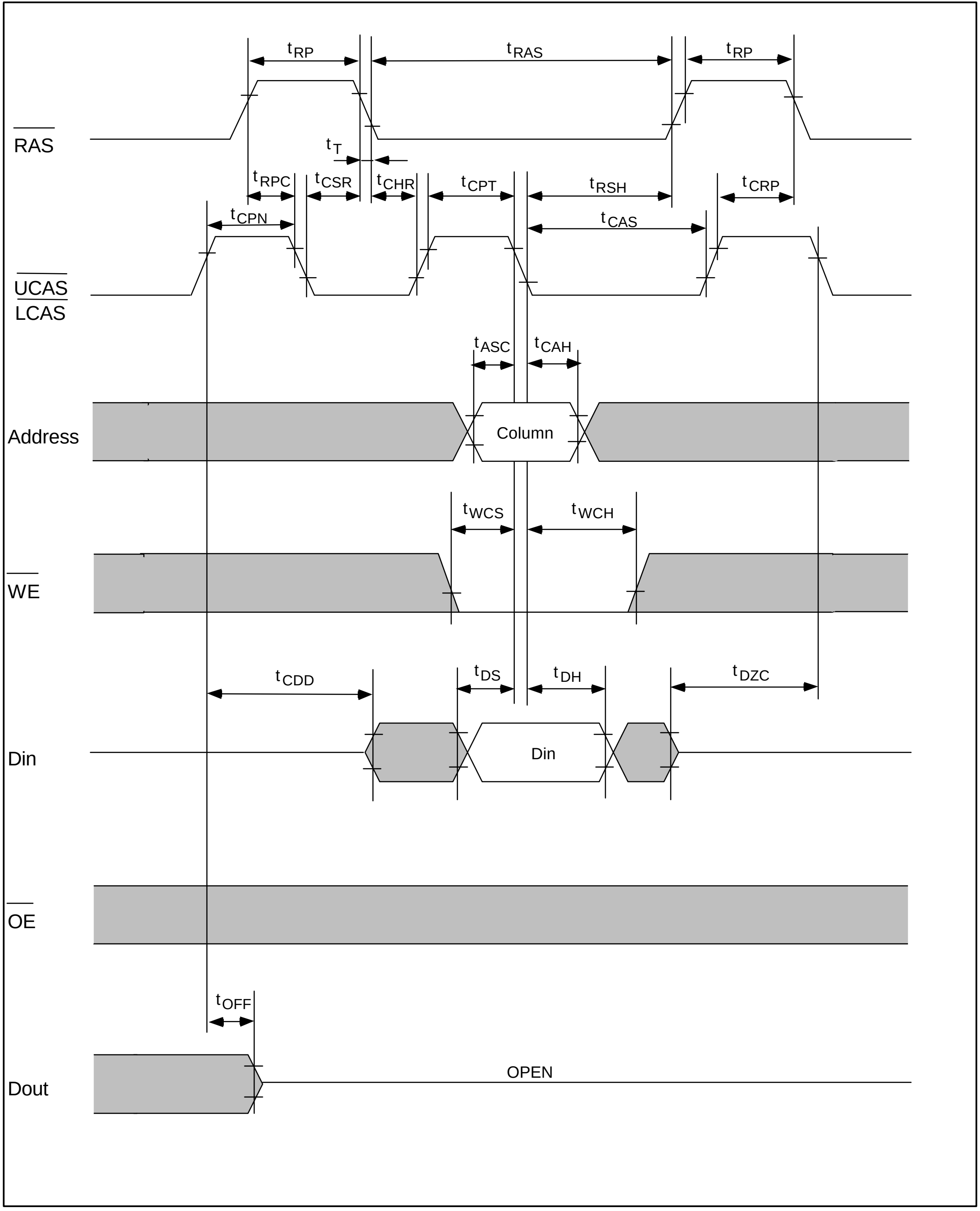
- CAS-Before-RAS Refresh Cycle



- Hidden Refresh Cycle

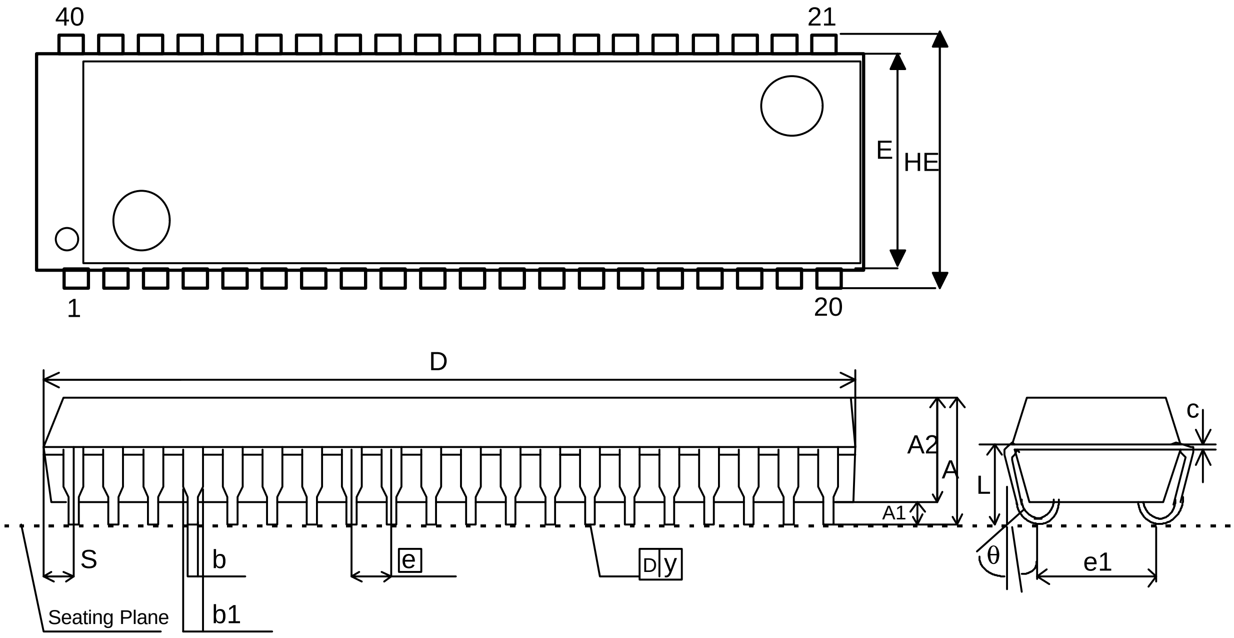


- $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Counter Check Cycle (WRITE)



Outline Drawing

40-Pin SOJ

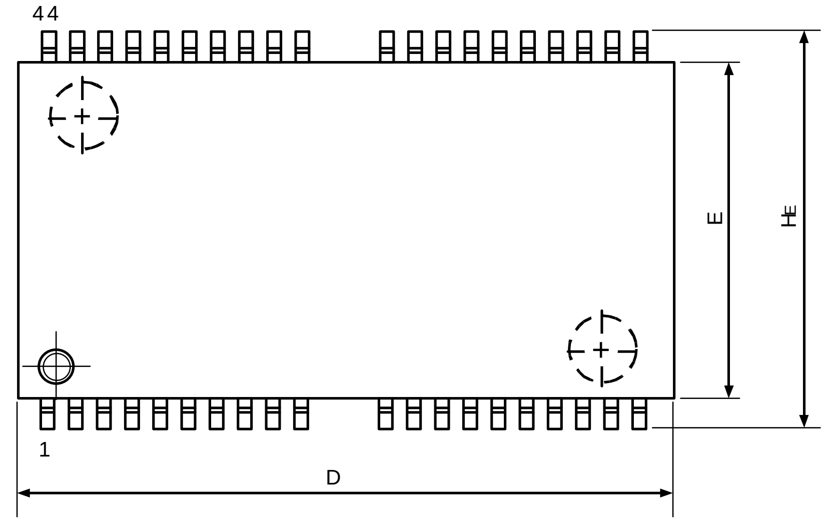


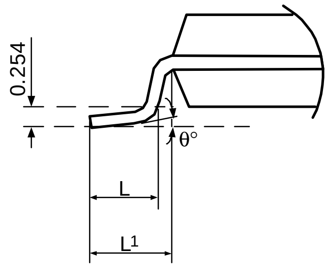
Symbol	**Dimension in inch**			**Dimension in mm**		
	Min	**Num**	**Max**	**Min**	**Num**	**Max**
A	-	-	0.144	-	-	3.66
A1	0.025	-	-	0.64	-	-
A2	0.105	0.110	0.115	2.67	2.79	2.92
b1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	-	1.025	1.035	-	26.04	26.29
E	0.395	0.400	0.405	10.03	10.16	10.29
$\boxed{e}$	0.044	0.050	0.056	1.12	1.2	1.42
e1	0.348	0.368	0.388	8.84	9.35	9.86
HE	0.430	0.440	0.450	10.92	11.18	11.43
L	0.088	0.098	0.108	2.24	2.49	2.74
S	-	-	0.050	-	-	1.27
Y	-	-	0.004	-	-	0.10
q	0°	-	10°	0°	-	10°

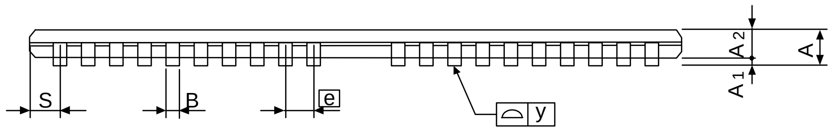
NOTE :

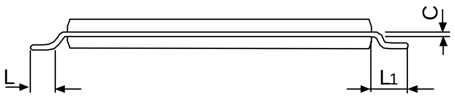
1. Dimension D Max & S include mold flash or tie bar burrs.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and are determined at the mold parting line.
4. Controlling dimension : inch
5. General appearance spec. should be based on final visual inspection spec.

40/44-Pin TSOP-II









Symbol	Dimension in inch			Dimension in mm		
	Min	Num	Max	Min	Num	Max
A	-	-	0.047	-	-	1.20
A1	0.002	-	-	0.05	-	-
A2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.010	0.014	0.018	0.25	0.35	0.45
c	-	0.006	-	-	0.15	-
D	0.721	0.725	0.729	18.31	18.41	18.51
E	0.396	0.400	0.404	10.06	10.16	10.26
e	-	0.031	-	-	0.80	-
HE	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	-	0.031	-	-	0.80	-
S	-	-	0.036	-	-	0.93
y	-	-	0.004	-	-	0.10
q	0°	-	5°	0°	-	5°

NOTE :

1. Dimension D&E do not include interiead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Dimension S includes end flash.
4. Controlling dimension : MM