Seven Stage Frequency Divider in I^2L Technique

triggerable by the positive flank of the input signal

Monolithic integrated circuit in I^2L technique designed primarily for use in electronic organs. The device incorporates seven flip-flops with externally accessible inputs and outputs. It is pin compatible with the SAJ 110 seven stage frequency divider.

The individual flip-flops can be interconnected to form a divider chain. Some flip-flop stages are already internally series-connected as shown below. The SAA 1004-N may be driven by sinusoidal as well as by square-wave input signals. The flip-flops change state with each positive-going flank of the input voltage (see Fig. 3).

Special features are: low impedance push-pull outputs, high input impedance, low current consumption and wide supply voltage operating range.

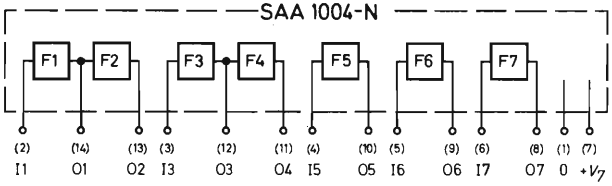
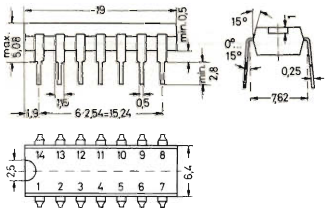


Fig. 1: Block diagram of the SAA 1004-N
The figures in brackets correspond to the pin numbers

Fig. 2:
SAA 1004-N in plastic package 20 A 14 according to DIN 41 866

Weight approximately 1.1 g
Dimensions in mm



All voltages are referred to pin 1.

Maximum Ratings

Supply voltage	V_7	15.5	V
Input voltage	V_I	$\leq V_7$	
Output current per stage	I_O	± 5	mA
Ambient operating temperature range	T_{amb}	$-10 \ldots +60$	°C
Storage temperature range	T_S	$-30 \ldots +125$	°C

Characteristics per Divider Stage at $V_7 = 9$ V, $R_L = 5.6$ kΩ, $T_{amb} = 25$ °C

Current consumption (unloaded)	I_7	0.8	mA
Input threshold voltage (see Fig. 4)	V_{IH}	6	V
	V_{IL}	2	V
Input resistance	r_i	40	kΩ
Output voltage high state R_L connected to pin 1	V_{OH}	$V_7 - 0.9$ V	
Output voltage low state R_L connected to pin 7	V_{OL}	0.3	V
Output resistance high state	r_H	100	Ω
Output resistance low state	r_L	200	Ω
Rise time of the output voltage	t_r	100	ns
Fall time of the output voltage	t_f	100	ns

Recommended Operating Conditions

Supply voltage	V_7	7 . . . 15	V
Input trigger voltage	V_{IH}	$> (V_7 - 1$ V)	
	V_{IL}	< 1	V
Load resistance at the output (connected to pin 1 or pin 7)	R_L	> 5.6	kΩ
Maximum input frequency	f_{max}	50	kHz

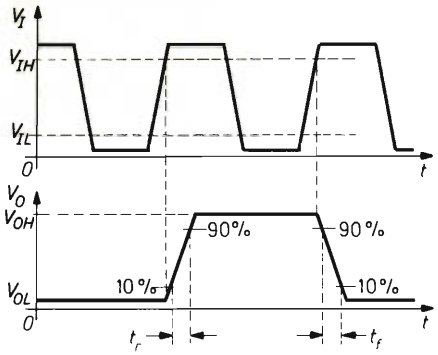


Fig. 3: Pulse diagram of a divider stage

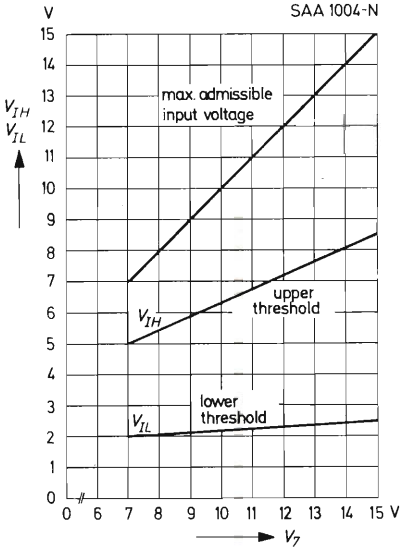


Fig. 4: Typical trigger range and admissible input voltage versus supply voltage