3602A, 3622A FAMILY
3602, 3622 FAMILY
2048 BIT (512×4) HIGH SPEED PROM

	3602A-2 3622A-2	3602A 3622A	3602 3622
Typ. T_A(ns)	45	55	60
Max. T_A(ns)	60	70	70

- **Low Power Dissipation --0.3mW/Bit**
- **Open Collector (3602A, 3602) or Three State (3622A, 3622) Outputs**
- **Simple Memory Expansion-- Chip Select Input Lead**
- **Replaces Two 256×4 PROMs Without Increasing Board Area**
- **Polycrystalline Silicon Fuse For Higher Reliability**
- **Hermetic 16-Pin DIP**

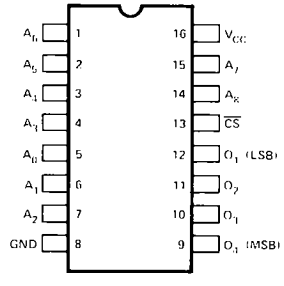
The Intel® 3602A/3622A and 3602/3622 device families are 2048-bit bipolar PROMs organized as 512 words by 4 bits. The fast second generation 3602A/3622A joins its Intel predecessor, the 3602/3622, featuring 70 ns. A higher speed version, the 3602A-2/3622A-2, is now available at 60 ns. All 3602A/3622A specifications, except programming, are the same as the 3602/3622. Once programmed, the 3602A/3622A are interchangeable with the 3602/3622.

The PROMs are manufactured with all outputs initially logically high. Logic low levels can be electrically programmed in selected bit locations. Both open collector and three-state outputs are available. The power dissipation is typically 0.3 mW/bit.

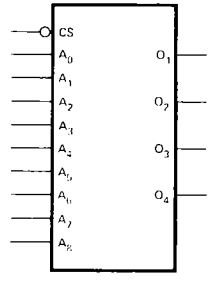
The pin configuration of the PROMs is the same as the popular 1K bit, 256 X 4 PROMs with the exception that CS_2 (pin 14) is address A_8. The bit density of existing 256 X 4 PROM systems can be easily doubled without an increase in area with the 3602A/3622A or 3602/3622. These PROMs, like the 256 X 4 PROMs, are in 16-pin dual in-line package.

A pin compatible, mask programmable 3302/3322 ROM is available for large volume production systems initially using the 3602/3622. Please contact Intel directly for details on these ROMs.

PIN CONFIGURATION



LOGIC SYMBOL



PROGRAMMING

The programming specifications are described in the PROM/ROM Programming Instructions on page 3-55.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1.6V to 5.6V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.[1]	Max.		
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	μA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	μA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_A = -10mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_S = -10mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15mA
I_{CEX}	Output Leakage Current			40	μA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC}	Power Supply Current		110	140	mA	V_{CC}=5.25V, V_{A0}→V_{A8} = 0V $\overline{CS}$ = 0V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

3622A, 3622A-2, 3622 ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			40	μA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}$=2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_{CC}=5.00V, T_A=25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC}=4.75V

NOTES: 1. Typical values are at 25° C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	MAX. LIMIT			UNIT	CONDITIONS
		3602A-2 3622A-2	3602A 3622A	3602 3622		
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	70	70	ns	$\overline{CS}$ = V_{IL} to Select the PROM
t_{S++}	Chip Select to Output Delay	30	30	30	ns	
t_{S--}	Chip Select to Output Delay	30	30	30	ns	

Capacitance [1] T_A = 25°C, f = 1 MHz

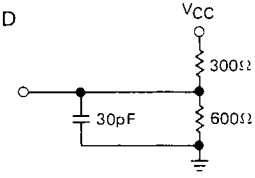
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS	
		TYP.	MAX.			
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	12	pF	V_{CC} = 5V	V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

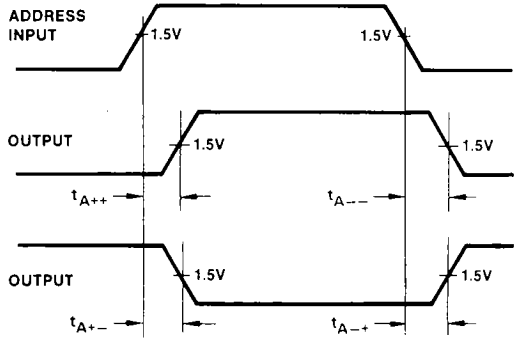
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD



Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY