3604A, 3624A AND 3604, 3624 FAMILY 4096 BIT (512×8) HIGH SPEED PROM

	3604A-2 3624A-2	3604A 3624A	3604AL	3604 3624	3604-4 3624-4	3604L-6
Max. T_A(ns)	60	70	90	70	90	90
Max. I_{CC}(mA)	175	175	130/25*	190	190	140/45*

***Standby Current When The Chip is Deselected.**

- **Fast Access Time --60ns Max (3604A-2, 3624A-2)**
- **Low Standby Power Dissipation (3604AL) --32μW/Bit Max**
- **Open Collector (3604A, 3604) or Three State (3624A, 3624) Outputs**
- **Four Chip Select Inputs For Easy Memory Expansion**
- **Polycrystalline Silicon Fuse For Higher Reliability**
- **Hermetic 24 Pin DIP**

The Intel® 3604A/3624A and 3604/3624 device families are 4096-bit bipolar PROMs organized as 512 words by 8 bits. The fast second generation 3604A/3624A joins its Intel predecessor, the 3604/3624, featuring 70 ns. Higher speed PROMs, the 3604A-2/3624A-2, are now available at 60 ns. The 3604A/3624A families are lower in power dissipation than the 3604/3624 families. All 3604A/3624A specifications, except programming, are the same as or better than the 3604/3624. Once programmed, the 3604A/3624A are interchangeable with the 3604/3624.

The PROMs are manufactured with all outputs initially logically high. Logic low levels can be electrically programmed in selected bit locations. Both open collector and three-state outputs are available. Low standby power dissipation can be achieved with either the 3604AL or 3604L-6. The standby power dissipation is approximately 15% of the active power dissipation.

The 3604A/3624A and 3604/3624 families are available in a hermetic 24-pin dual in-line package. These PROMs are manufactured with the time-proven polycrystalline silicon fuse technology. A pin compatible, mask programmable ROM is available for large volume production of systems initially using the 3604/3624. Please contact Intel directly for details on these ROMs.

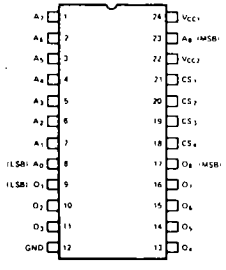
Mode/Pin Connection		Pin 22	Pin 24
READ:	3604A, 3604A-2, 3604, 3604-4, 3624A, 3624A-2, 3624, 3624-4	No Connect or 5V	5V
	3604AL, 3604L-6	+5V	Must be Left Open
PROGRAM:	3604A, 3604A-2, 3604, 3604-4, 3624A, 3624A-2, 3624, 3624-4	Pulsed 12.5V	Pulsed 12.5V
	3604AL, 3604L-6	Pulsed 12.5V	Pulsed 12.5V
STANDBY:	3604AL, 3604L-6	Power dissipation is automatically reduced whenever the 3604AL or 3604L-6 is deselected.	

PIN NAMES

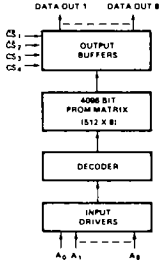
A_0–A_8	ADDRESS INPUTS
$\overline{CS}_1$–$\overline{CS}_2$, CS_3–CS_4 [1]	CHIP SELECT INPUTS
O_1–O_8	DATA OUTPUTS

[1] To select the PROM $\overline{CS}_1 = \overline{CS}_2 = 0$ and $CS_3 = CS_4 = 1$.

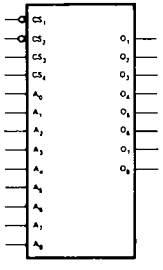
PIN CONFIGURATION



BLOCK DIAGRAM



LOGIC SYMBOL



PROGRAMMING

The programming specifications are described in the PROM/ROM Programming Instructions on page 3-55.

Absolute Maximum Ratings*

Temperature Under Bias . . . . . -65°C to +125°C
Storage Temperature . . . . . -65°C to +160°C
Output or Supply Voltages . . . . . -0.5V to 7 Volts
All Input Voltages . . . . . -1.6 to 5.5V
Output Currents 100mA

*COMMENT

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

D. C. Characteristics: All Limits Apply for V_{CC} = +5.0V ±5%, T_A = 0°C to +75°C

Symbol	Parameter	Limits Min.	Typ.[1]	Max.	Unit	Test Conditions
I_{FA}	Address Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_A = 0.45V
I_{FS}	Chip Select Input Load Current		-0.05	-0.25	mA	V_{CC} = 5.25V, V_S = 0.45V
I_{RA}	Address Input Leakage Current			40	µA	V_{CC} = 5.25V, V_A = 5.25V
I_{RS}	Chip Select Input Leakage Current			40	µA	V_{CC} = 5.25V, V_S = 5.25V
V_{CA}	Address Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_A = -10 mA
V_{CS}	Chip Select Input Clamp Voltage		-0.9	-1.5	V	V_{CC} = 4.75V, I_S = -10 mA
V_{OL}	Output Low Voltage		0.3	0.45	V	V_{CC} = 4.75V, I_{OL} = 15 mA
I_{CEX}	Output Leakage Current			100	µA	V_{CC} = 5.25V, V_{CE} = 5.25V
I_{CC1}	Power Supply Current (3604A, 3604A-2, 3624A, and 3624A-2)		130	175	mA	V_{CC1} = 5.25V, V_{A0}→V_{A8} = 0V, $\overline{CS}_1 = \overline{CS}_2$ = 0V, $CS_3 = CS_4$ = 5.25V
I_{CC2}	Power Supply Current (3604, 3604-4, 3624, and 3624-4)		160	190	mA	V_{CC1} = 5.25V, V_{A0}→V_{A8} = 0V, $\overline{CS}_1 = \overline{CS}_2$ = 0V, $CS_3 = CS_4$ = 5.25V
I_{CC3}	Power Supply Current (3604AL) Active		100	130	mA	V_{CC2} = 5.25V, V_{CC1} = Open $\overline{CS}_1 = \overline{CS}_2$ = 0.45V, $CS_3 = CS_4$ = 2.4V
	Standby		15	25	mA	$\overline{CS}_1 = \overline{CS}_2$ = 2.5V
I_{CC4}	Power Supply Current (3604L-6) Active			140	mA	V_{CC2} = 5.25V, V_{CC1} = Open $\overline{CS}_1 = \overline{CS}_2$ = 0.45V, $CS_3 = CS_4$ = 2.4V
	Standby			45	mA	$\overline{CS}_1 = \overline{CS}_2$ = 2.5V
V_{IL}	Input "Low" Voltage			0.85	V	V_{CC} = 5.0V
V_{IH}	Input "High" Voltage	2.0			V	V_{CC} = 5.0V

3624A AND 3624 FAMILY ONLY

Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Test Conditions
$\|I_O\|$	Output Leakage for High Impedance Stage			100	µA	V_O=5.25V or 0.45V, V_{CC}=5.25V, $\overline{CS}_1 = \overline{CS}_2$=2.4V
I_{SC}[2]	Output Short Circuit Current	-15	-25	-60	mA	V_{CC}=5.00V, T_A=25°C, V_O = 0V
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-2.4mA, V_{CC} = 4.75V

NOTES: 1. Typical values are at 25° C and at nominal voltage.
2. Unmeasured outputs are open during this test.

A. C. Characteristics V_{CC} = +5V ±5%, T_A = 0°C to +75°C

SYMBOL	PARAMETER	3604A, 3624A FAMILY MAXIMUM LIMITS (ns)			3064, 3624 FAMILY MAXIMUM LIMITS (ns)		
		3604A-2 3624A-2	3604A 3624A	3604AL	3064 3624	3604-4 3624-4	3604L-6
t_{A++}, t_{A--} t_{A+-}, t_{A-+}	Address to Output Delay	60	70	90	70	90	90
t_{S++}	Chip Select to Output Delay	30	30	30	30	30	30
t_{S--}	Chip Select to Output Delay	30	30	120	30	30	120

Capacitance [1] T_A = 25°C, f = 1 MHz

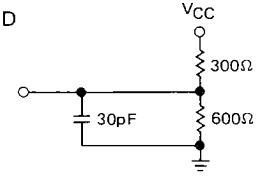
SYMBOL	PARAMETER	LIMITS		UNIT	TEST CONDITIONS	
		TYP.	MAX.			
C_{INA}	Address Input Capacitance	4	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{INS}	Chip-Select Input Capacitance	6	10	pF	V_{CC} = 5V	V_{IN} = 2.5V
C_{OUT}	Output Capacitance	7	15	pF	V_{CC} = 5V	V_{OUT} = 2.5V

NOTE 1: This parameter is only periodically sampled and is not 100% tested.

Switching Characteristics

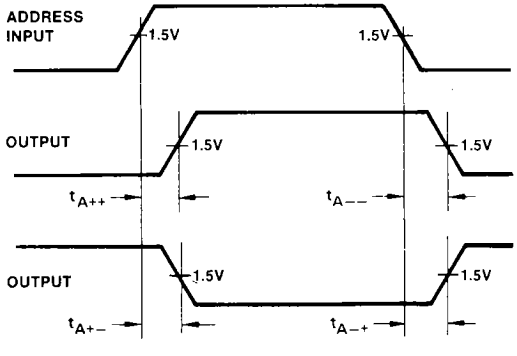
Conditions of Test:
Input pulse amplitudes - 2.5V
Input pulse rise and fall times of
5 nanoseconds between 1 volt and 2 volts
Speed measurements are made at 1.5 volt levels
Output loading is 15 mA and 30 pF
Frequency of test - 2.5 MHz

15 mA TEST LOAD



Waveforms

ADDRESS TO OUTPUT DELAY



CHIP SELECT TO OUTPUT DELAY