Schottky Bipolar 8216/8226

4 BIT PARALLEL BIDIRECTIONAL BUS DRIVER

- Data Bus Buffer Driver for 8080 CPU
- Low Input Load Current .25 mA Maximum
- High Output Drive Capability for Driving System Data Bus
- 3.65V Output High Voltage for Direct Interface to 8080 CPU
- Three State Outputs
- Reduces System Package Count

The 8216/8226 is a 4-bit bi-directional bus driver/receiver.

All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V V_{OH} , and for high capacitance terminated bus structures, the DB outputs provide a high 50mA I_{OL} capability.

A non-inverting (8216) and an inverting (8226) are available to meet a wide variety of applications for buffering in microcomputer systems.



FUNCTIONAL DESCRIPTION

Microprocessors like the 8080 are MOS devices and are generally capable of driving a single TTL load. The same is true for MOS memory devices. While this type of drive is sufficient in small systems with few components, quite often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multi-board system.

The 8216/8226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bi-Directional Driver

Each buffered line of the four bit driver consists of two separate buffers that are tri-state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this side is used to interface to the system side components such as memories, I/O, etc., because its interface is direct TTL compatible and it has high drive (50mA). On the other side of the driver the inputs and outputs are separated to provide maximum flexibility. Of course, they can be tied together so that the driver can be used to buffer a true bi-directional bus such as the 8080 Data Bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65V) so that direct interface to the 8080 and 8008 CPUs is achieved with an adequate amount of noise immunity (350mV worst case).

Control Gating DIEN, CS

The \overline{CS} input is actually a device select. When it is "high" the output drivers are all forced to their high-impedance state. When it is at "zero" the device is selected (enabled) and the direction of the data flow is determined by the \overline{DIEN} input.

The $\overline{\text{DIEN}}$ input controls the direction of data flow (see Figure 1) for complete truth table. This direction control is accomplished by forcing one of the pair of buffers into its high impedance state and allowing the other to transmit its data. A simple two gate circuit is used for this function.

The 8216/8226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.



(a) 8216



Figure 1. 8216/8226 Logic Diagrams

APPLICATIONS OF 8216/8226

8080 Data Bus Buffer

The 8080 CPU Data Bus is capable of driving a single TTL load and is more than adequate for small, single board systems. When expanding such a system to more than one board to increase I/O or Memory size, it is necessary to provide a buffer. The 8216/8226 is a device that is exactly fitted to this application.

Shown in Figure 2 are a pair of 8216/8226 connected directly to the 8080 Data Bus and associated control signals. The buffer is bi-directional in nature and serves to isolate the CPU data bus.

On the system side, the DB lines interface with standard semiconductor I/O and Memory components and are completely TTL compatible. The DB lines also provide a high drive capability (50mA) so that an extremely large system can be dirven along with possible bus termination networks.

On the 8080 side the DI and DO lines are tied together and are directly connected to the 8080 Data Bus for bi-directional operation. The DO outputs of the 8216/8226 have a high voltage output capability of 3.65 volts which allows direct connection to the 8080 whose minimum input voltage is 3.3 volts. It also gives a very adequate noise margin of 350mV (worst case).

The DIEN inputs to 8216/8226 is connected directly to the 8080. DIEN is tied to DBIN so that proper bus flow is maintained, and \overline{CS} is tied to \overline{BUSEN} so that the system side Data Bus will be 3-stated when a Hold request has been acknowledged during a DMA activity.

Memory and I/O Interface to a Bi-directional Bus

In large microcomputer systems it is often necessary to provide Memory and I/O with their own buffers and at the same time maintain a direct, common interface to a bi-directional Data Bus. The 8216/8226 has separated data in and data out lines on one side and a common bi-directional set on the other to accomodate such a function.

Shown in Figure 3 is an example of how the 8216/8226 is used in this type of application.

The interface to Memory is simple and direct. The memories used are typically Intel[®] 8102, 8102A, 8101 or 8107B-4 and have separate data inputs and outputs. The DI and DO lines of the 8216/8226 tie to them directly and under control of the $\overline{\text{MEMR}}$ signal, which is connected to the $\overline{\text{DIEN}}$ input, an interface to the bi-directional Data Bus is maintained.

The interface to I/O is similar to Memory. The I/O devices used are typically $Intel^{(8)}$ 8255s, and can be used for both input and output ports. The I/O R signal is connected directly to the DIEN input so that proper data flow from the I/O device to the Data Bus is maintained.

The 8216/8226 can be used in a wide variety of other buffering functions in microcomputer systems such as Address Bus Drivers, Drivers to peripheral devices such as printers, and as Drivers for long length cables to other peripherals or systems.



Figure 2. 8080 Data Bus Buffer.



Figure 3. Memory and I/O Interface to a Bi-Directional Bus.

D.C. AND OPERATING CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias	
Storage Temperature	65°C to +150°C
All Output and Supply Voltages	
All Input Voltages	1.0V to +5.5V
Output Currents	125 mA

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied.

				Limits				
Symbol	Parameter		Min.	Тур.	Max.	Unit	Conditions	
I _{F1}	Input Load Current DIE		-0.15	5	mA	V _F = 0.45		
I _{F2}	Input Load Current All	S	-0.08	25	mA	V _F = 0.45		
I _{R1}	Input Leakage Current			20	μA	V _R = 5.25V		
I _{R2}	Input Leakage Current			10	μA	V _R = 5.25V		
V _C	Input Forward Voltage			-1	V	I _C = -5mA		
VIL	Input "Low" Voltage				.95	V		
VIH	Input "High" Voltage		2.0			V		
I _O	Output Leakage Curren (3-State)	t Di	D B		20 100	μΑ	V _O = 0.45V/5.25V	
	I _{CC} Power Supply Current	8216		95	130	mA		
ICC		8226		85	120	mA		
V _{OL1}	Output "Low" Voltage			0.3	.45	V	DO Outputs I _{OL} =15mA DB Outputs I _{OL} =25mA	
V _{OL2}	Output "Low" Voltage 8216 8226		0.5	.6	V	DB Outputs I _{OL} =55mA		
			0.5	.6	V	DB Outputs I _{OL} =50mA		
V _{OH1}	Output "High" Voltage		3.65	4.0		V	DO Outputs I _{OH} = -1mA	
V _{OH2}	Output "High" Voltage		2.4	3.0		V	DB Outputs I _{OH} = -10mA	
los	Output Short Circuit Cu	urrent	-15 -30	-35 -75	-65 -120	mA mA	DO Outputs $V_0 \cong 0V$, DB Outputs $V_{CC}=5.0V$	

$T_A = 0^{\circ}C$ to +70°C, V_{CC} =+5V ±5%

NOTE: Typical values are for $T_A = 25^{\circ}$ C, $V_{CC} = 5.0$ V.

SCHOTTKY BIPOLAR 8216/8226





A.C. CHARACTERISTICS

 $T_A = 0^{\circ}C$ to +70°C, $V_{CC} = +5V \pm 5\%$

		Limits					
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	Conditions	
T _{PD1}	Input to Output Delay DO Outputs		15	25	ns	C _L =30pF, R ₁ =300Ω R ₂ =600Ω	
T _{PD2}	Input to Output Delay DB Outputs						
	8216		20	30	ns	C _L =300pF, R ₁ =90Ω	
	8226		16	25	ns	R ₂ = 180Ω	
Τ _Ε	Output Enable Time						
	8216		45	65	ns	(Note 2)	
	8226		35	54	ns	(Note 3)	
T_D	Output Disable Time		20	35	ns	(Note 4)	

TEST CONDITIONS:

Input pulse amplitude of 2.5V. Input rise and fall times of 5 ns between 1 and 2 volts. Output loading is 5 mA and 10 pF. Speed measurements are made at 1.5 volt levels.



Capacitance^[5]

			Limits			
Symbol	Parameter	Min.	Typ.[1]	Max.	Unit	
C _{IN}	Input Capacitance		4	8	pF	
C _{OUT1}	Output Capacitance		6	10	pF	
C _{OUT2}	Output Capacitance		13	18	pF	

TEST CONDITIONS: $V_{BIAS} = 2.5V$, $V_{CC} = 5.0V$, $T_A = 25^{\circ}C$, f = 1 MHz.

NOTES: 1. Typical values are for $T_A = 25^{\circ}C$, $V_{CC} = 5.0V$.

2. DO Outputs, $C_L = 30pF$, $R_1 = 300/10 \text{ K}\Omega$, $R_2 = 180/1\text{ K}\Omega$; DB Outputs, $C_L = 300pF$, $R_1 = 90/10 \text{ K}\Omega$, $R_2 = 180/1 \text{ K}\Omega$.

- 3. DO Outputs, $C_L = 30pF$, $R_1 = 300/10 \text{ K}\Omega$, $R_2 = 600/1\text{ K}$; DB Outputs, $C_L = 300pF$, $R_1 = 90/10 \text{ K}\Omega$, $R_2 = 180/1 \text{ K}\Omega$.
- 4. DO Outputs, $C_L = 5pF$, $R_1 = 300/10 \text{ K}\Omega$, $R_2 = 600/1 \text{ K}\Omega$; DB Outputs, $C_L = 5pF$, $R_1 = 90/10 \text{ K}\Omega$, $R_2 = 180/1 \text{ K}\Omega$.
- 5. This parameter is periodically sampled and not 100% tested.