256K x 16 FAST PAGE MODE CMOS DYNAMIC RAM

HIGH PERFORMANCE	40	45	50	60
Max. $\overline{RAS}$ Access Time, (t_{RAC})	40 ns	45 ns	50 ns	60 ns
Max. Column Address Access Time, (t_{CAA})	20 ns	22 ns	24 ns	30 ns
Min. Fast Page Mode Cycle Time, (t_{PC})	23 ns	25 ns	28 ns	35 ns
Min. Read/Write Cycle Time, (t_{RC})	75 ns	80 ns	90 ns	110 ns

Features

- 256K x 16-bit organization
- Fast Page Mode for a sustained data rate of 43 MHz.
- $\overline{RAS}$ access time: 40, 45, 50, 60 ns
- Dual $\overline{CAS}$ Inputs
- Low power dissipation
- Read-Modify-Write, $\overline{RAS}$-Only Refresh, $\overline{CAS}$-Before-$\overline{RAS}$ Refresh
- Refresh Interval: 512 cycles/8 ms
- Available in 40-pin 400 mil SOJ and 40/44L-pin 400 mil TSOP-II packages
- Single +5V ±10% Power Supply
- TTL Interface

Description

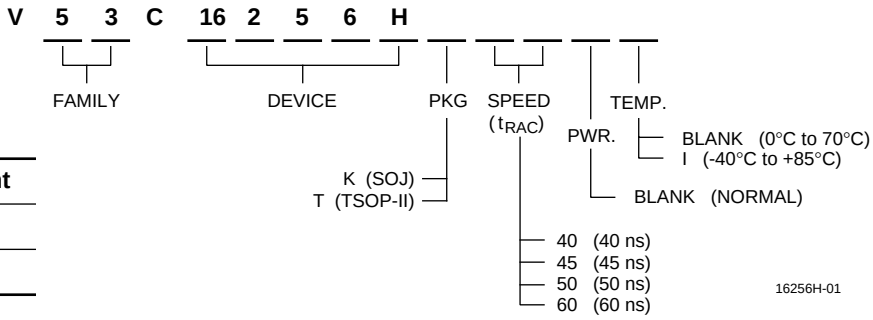
The V53C16256H is a 262,144 x 16 bit high-performance CMOS dynamic random access memory. The V53C16256H offers Fast Page mode with dual $\overline{CAS}$ inputs. An address, $\overline{CAS}$ and $\overline{RAS}$ input capacitances are reduced to one quarter when the x4 DRAM is used to construct the same memory density. The V53C16256H has symmetric address and accepts 512 cycle 8ms interval.

All inputs are TTL compatible. Fast Page Mode operation allows random access up to 512 x 16 bits, within a page, with cycle times as short as 23ns.

The V53C16256H is best suited for graphics, and DSP applications.

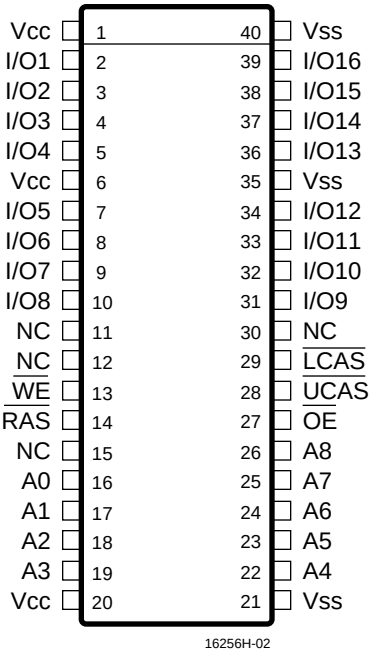
Device Usage Chart

Operating Temperature Range	Package Outline		Access Time (ns)				Power	Temperature Mark
	K	T	40	45	50	60	Std.	
0°C to 70 °C	•	•	•	•	•	•	•	Blank
-40°C to +85°C	•	•	•	•	•	•	•	I

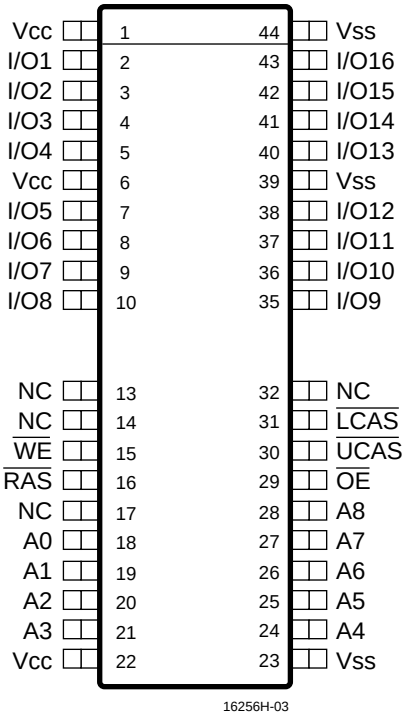


Description	Pkg.	Pin Count
SOJ	K	40
TSOP-II	T	40/44L

40-Pin Plastic SOJ PIN CONFIGURATION Top View



40/44 Pin Plastic TSOP-II PIN CONFIGURATION Top View



Pin Names

A_0–A_8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{UCAS}$	Column Address Strobe Upper Byte Control
$\overline{LCAS}$	Column Address Strobe Lower Byte Control
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
I/O_1–I/O_{16}	Data Input, Output
V_{CC}	+5V Supply
V_{SS}	0V Supply
NC	No Connect

*Absolute Maximum Ratings**

Ambient Temperature
Under Bias ..... –10°C to +80°C
Storage Temperature (plastic) ..... –55°C to +125°C
Voltage Relative to V_{SS} .....–1.0 V to +7.0V
Data Output Current ..... 50 mA
Power Dissipation ..... 1.0 W

***Note:** Operation above Absolute Maximum Ratings can adversely affect device reliability.

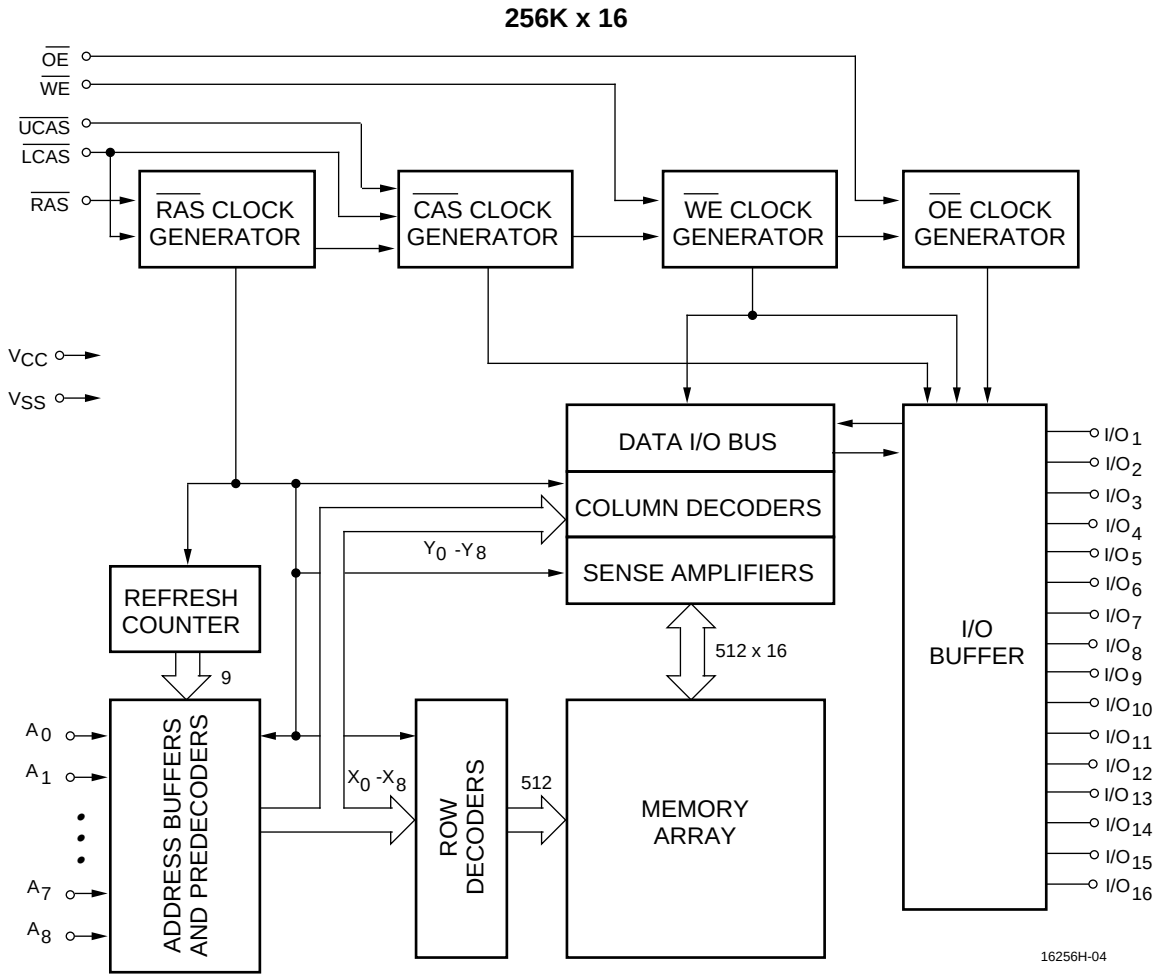
*Capacitance**

T_A = 25°C, V_{CC} = 5V ± 10%, V_{SS} = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C_{IN1}	Address Input	3	4	pF
C_{IN2}	$\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$, $\overline{WE}$, $\overline{OE}$	4	5	pF
C_{OUT}	Data Input/Output	5	7	pF

*** Note:** Capacitance is sampled and not 100% tested

Block Diagram



DC and Operating Characteristics (1-2)

T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Access Time	V53C16256H			Unit	Test Conditions	Notes
			Min.	Typ.	Max.			
I_{LI}	Input Leakage Current (any input pin)		–10		10	µA	$V_{SS} \le V_{IN} \le V_{CC}$	
I_{LO}	Output Leakage Current (for High-Z State)		–10		10	µA	$V_{SS} \le V_{OUT} \le V_{CC}$ $\overline{RAS}$, $\overline{CAS}$ at V_{IH}	
I_{CC1}	V_{CC} Supply Current, Operating	40			200	mA	$t_{RC} = t_{RC}$ (min.)	1, 2
		45			190			
		50			180			
		60			170			
I_{CC2}	V_{CC} Supply Current, TTL Standby				2	mA	$\overline{RAS}$, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
I_{CC3}	V_{CC} Supply Current, $\overline{RAS}$-Only Refresh	40			200	mA	$t_{RC} = t_{RC}$ (min.)	2
		45			190			
		50			180			
		60			170			
I_{CC4}	V_{CC} Supply Current, Fast Page Mode Operation	40			190	mA	Minimum Cycle	1, 2
		45			180			
		50			170			
		60			160			
I_{CC5}	V_{CC} Supply Current, Standby, Output Enabled other inputs ≥ V_{SS}				2	mA	$\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$	1
I_{CC6}	V_{CC} Supply Current, CMOS Standby				1	mA	$\overline{RAS} \ge V_{CC} - 0.2$ V, $\overline{CAS} \ge V_{CC} - 0.2$ V, All other inputs ≥ V_{SS}	
V_{IL}	Input Low Voltage		–1		0.8	V		3
V_{IH}	Input High Voltage		2.4		V_{CC} + 1	V		3
V_{OL}	Output Low Voltage				0.4	V	I_{OL} = 2.0 mA	
V_{OH}	Output High Voltage		2.4			V	I_{OH} = –2.0 mA	

AC Characteristics

Over all temperature range, V_{CC} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	40		45		50		60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	40	75	45	75K	50	75K	60	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	75		80		90		110		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	25		25		30		40		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	40		45		50		60		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	12		13		14		15		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	17	28	18	32	19	36	20	45	ns	
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		0		ns	4
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	7		8		9		10		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	5		6		7		10		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH\ (R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	12		13		14		15		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		5		5		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		0		ns	5
16	$t_{OEL1RH2}$	t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	8		9		10		10		ns	
17	t_{GL1QV}	t_{OAC}	Access Time from $\overline{OE}$		12		13		14		15	ns	
18	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		12		13		14		15	ns	6, 7
19	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		45		50		55		60	ns	6, 8, 9
20	t_{AVQV}	t_{CAA}	Access Time from Column Address		20		22		24		30	ns	6, 7, 10
21	t_{CL1QX}	t_{LZ}	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		0		ns	16
22	t_{CH2QZ}	t_{HZ}	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	6	0	7	0	8	0	10	ns	16
23	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	30		35		40		50		ns	
24	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	12	20	13	23	14	26	15	30	ns	11
25	$t_{CL1RH1(W)}$	$t_{RSH\ (W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	12		13		14		15		ns	
26	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	12		13		14		15		ns	
27	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		0		ns	12, 13
28	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	5		6		7		10		ns	

AC Characteristics (Cont'd)

#	JEDEC Symbol	Symbol	Parameter	40		45		50		60		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
29	t_{WL1WH1}	t_{WP}	Write Pulse Width	5		6		7		10		ns	
30	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	30		35		40		50		ns	
31	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	12		13		14		15		ns	
32	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		0		ns	14
33	t_{WL1DX}	t_{DH}	Data in Hold Time	5		6		7		10		ns	14
34	t_{WL1GL2}	t_{WOH}	Write to $\overline{OE}$ Hold Time	6		7		8		10		ns	14
35	t_{GH2DX}	t_{OED}	$\overline{OE}$ to Data Delay Time	6		7		8		10		ns	14
36	t_{RL2RL2} (RMW)	t_{RWC}	Read-Modify-Write Cycle Time	110		115		130		170		ns	
37	t_{RL1RH1} (RMW)	t_{RRW}	Read-Modify-Write Cycle $\overline{RAS}$ Pulse Width	75		80		87		105		ns	
38	t_{CL1WL2}	t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	30		32		34		40		ns	12
39	t_{RL1WL2}	t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay in Read-Modify-Write Cycle	58		62		68		85		ns	12
40	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	48		50		52		65		ns	
41	t_{AVWL2}	t_{AWD}	Col. Address to $\overline{WE}$ Delay	38		41		42		58		ns	12
42	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	23		25		28		35		ns	
43	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	5		6		7		10		ns	
44	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	20		22		24		30		ns	
45	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		22		24		27		34	ns	7
46	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	30		35		40		50		ns	
47	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		10		ns	
48	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	0		0		0		0		ns	
49	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	8		10		12		15		ns	
50	t_{CL2CL2} (RMW)	t_{PCM}	Fast Page Mode Read-Modify-Write Cycle Time	60		65		70		85		ns	
51	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	3	50	ns	15
52		t_{REF}	Refresh Interval (512 Cycles)	8			8		8		8	ms	17

Notes:

1. I_{CC} is dependent on output loading when the device output is selected. Specified I_{CC} (max.) is measured with the output open.
2. I_{CC} is dependent upon the number of address transitions. Specified I_{CC} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to –1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{CC}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to one TTL input and 50 pF.
7. Access time is determined by the longest of t_{CAA}, t_{CAC} and t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 3 ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

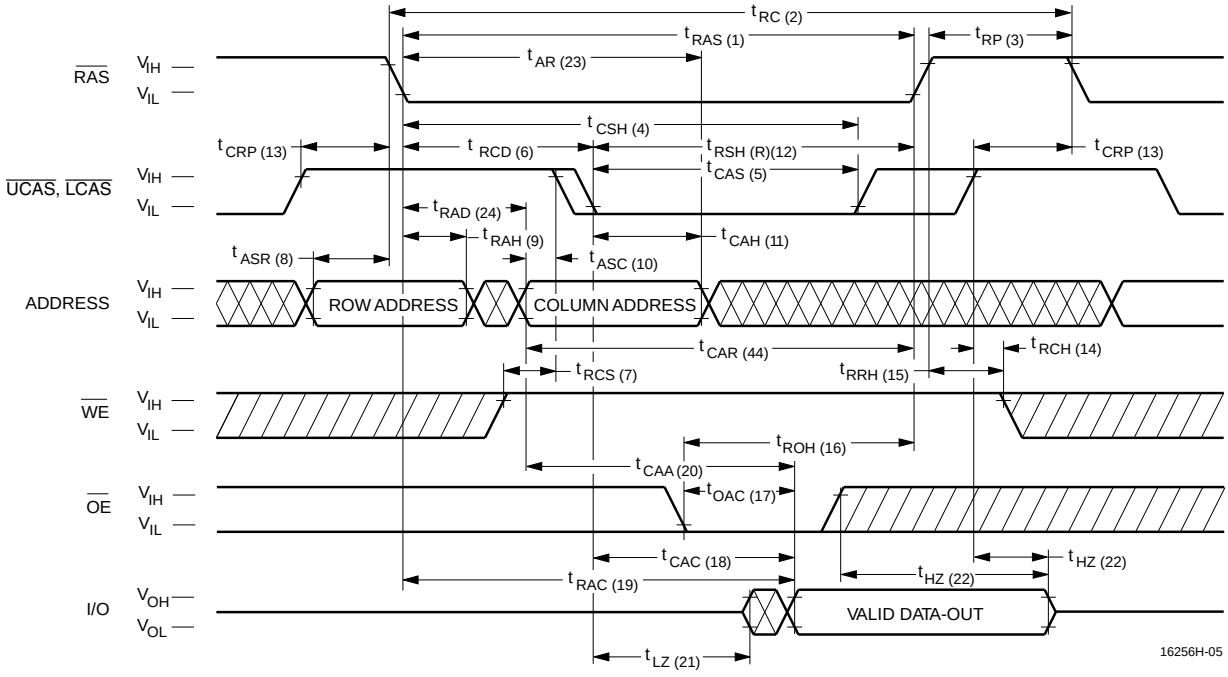
Truth Table

Function	$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESS	I/O	Notes
Standby	H	H	H	X	X		High-Z	
Read: Word	L	L	L	H	L	ROW/COL	Data Out	
Read: Lower Byte	L	L	H	H	L	ROW/COL	Lower Byte, Data-Out Upper Byte, High-Z	
Read: Upper Byte	L	H	L	H	L	ROW/COL	Lower Byte, High-Z Upper Byte, Data-Out	
Write: Word (Early-Write)	L	L	L	L	X	ROW/COL	Data-In	
Write: Lower Byte (Early)	L	L	H	L	X	ROW/COL	Lower Byte, Data-In Upper Byte, High-Z	
Read: Upper Byte (Early)	L	H	L	L	X	ROW/COL	Lower Byte, High-Z Upper Byte, Data-In	
Read-Write	L	L	L	H→L	L→H	ROW/COL	Data-Out, Data-In	1, 2
Page-Mode Read	L	H→L	H→L	H	L	COL	Data-Out	2
Page-Mode Write	L	H→L	H→L	L	X	COL	Data-In	2
Page-Mode Read-Write	L	H→L	H→L	H→L	L→H	COL	Data-Out, Data-In	1, 2
Hidden Refresh Read	L→H→L	L	L	H	L	ROW/COL	Data-Out	2
$\overline{RAS}$-Only Refresh	L	H	H	X	X	ROW	High-Z	
CBR Refresh	H→L	L	L	X	X		High-Z	3

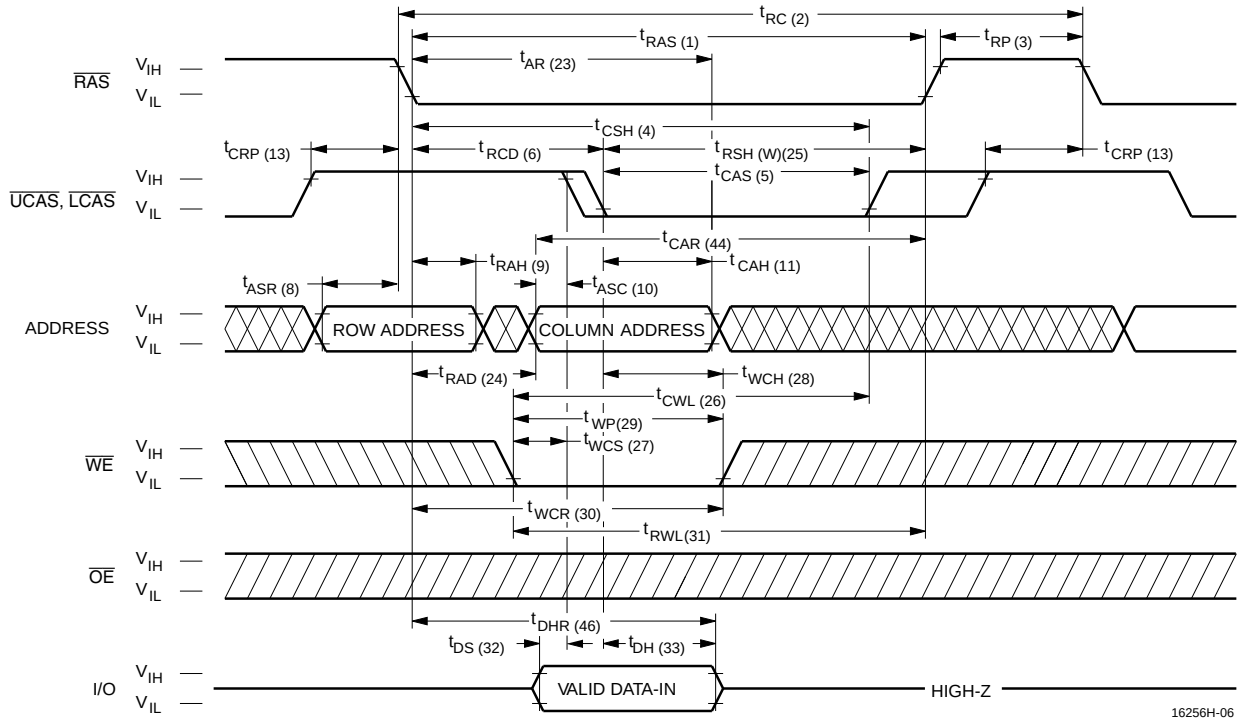
Notes:

1. Byte Write cycles $\overline{LCAS}$ or $\overline{UCAS}$ active.
2. Byte Read cycles $\overline{LCAS}$ or $\overline{UCAS}$ active.
3. Only one of the two $\overline{CAS}$ must be active ($\overline{LCAS}$ or $\overline{UCAS}$).

Waveforms of Read Cycle

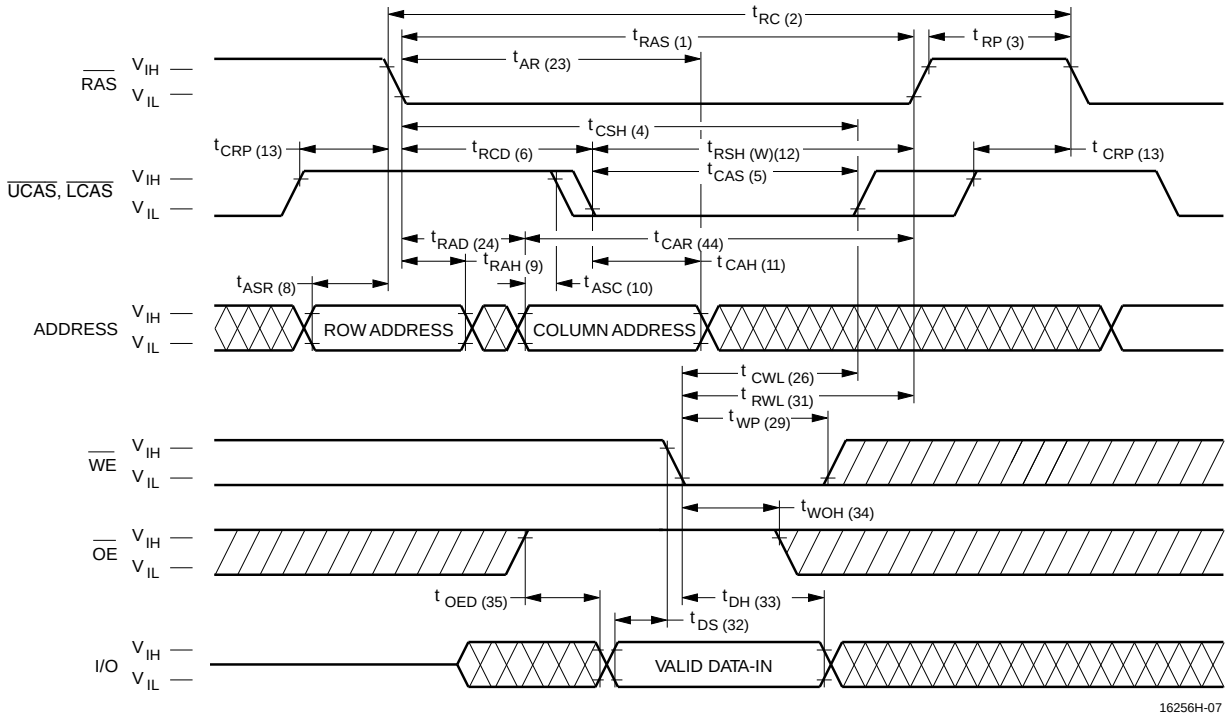


Waveforms of Early Write Cycle

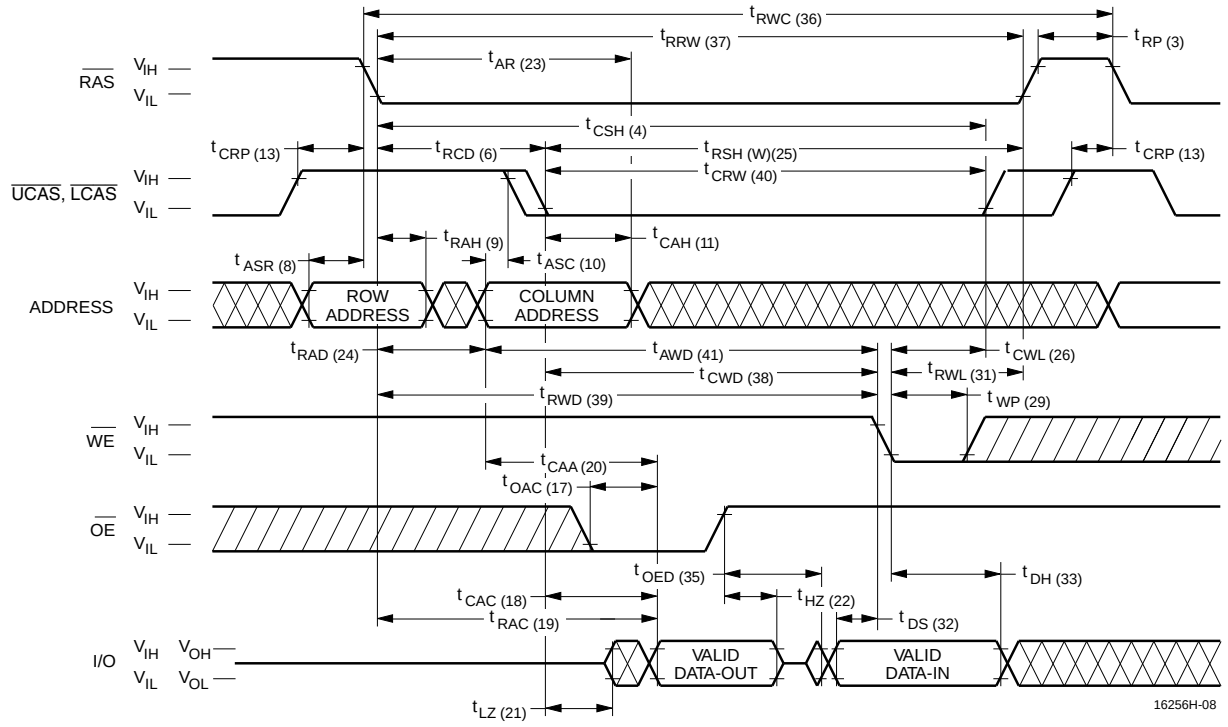


Don't Care Undefined

Waveforms of $\overline{OE}$-Controlled Write Cycle



Waveforms of Read-Modify-Write Cycle



Don't Care Undefined