

MOS INTEGRATED CIRCUITS



PRELIMINARY DATA

TONE GENERATOR

- SINGLE POWER SUPPLY
- WIDE SUPPLY VOLTAGE OPERATING RANGE
- LOW POWER DISSIPATION < 500 mW
- 13 (M082/A, M083/A) OR 12 (M086/A) TONE OUTPUTS
- HIGH OUTPUT DRIVE CAPABILITY
- HIGH ACCURACY OF OUTPUT FREQUENCIES: ERROR LESS THAN \pm 0.069%
- INPUT PROTECTED AGAINST STATIC CHARGES
- LOW INTERMODULATION

The M082/A, M083/A and M086/A are monolithic tone generators specifically designed for electronic organs. The only difference between the M082, M083, M086 and the M082A, M083A, M086A is the maximum input clock frequency, which is 4500 KHz for the standard types and 2500 KHz for the "A" types. Constructed on a single chip using low threshold N-channel silicon gate technology they are supplied in a 16 lead dual in-line plastic package.

ABSOLUTE MAXIMUM RATINGS *

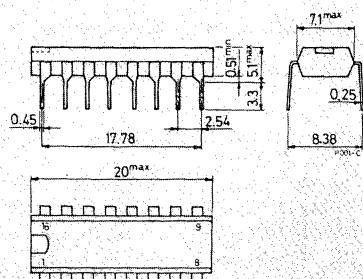
V_i	Voltage on any pin relative to V_{SS} (GND)	+20 to -0.3	V
T_{op}	Operating temperature	0 to 50	°C
T_{stg}	Storage temperature	-65 to 150	°C

* Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

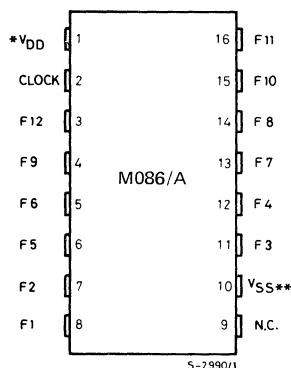
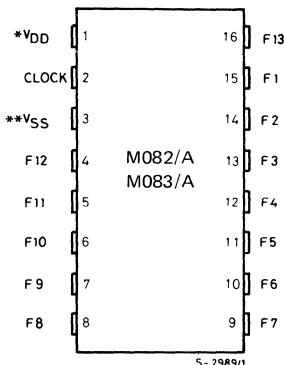
ORDERING NUMBERS: M082B1 M082A B1
 M083B1 M083A B1
 M086B1 M086A B1

MECHANICAL DATA

Dimensions in mm



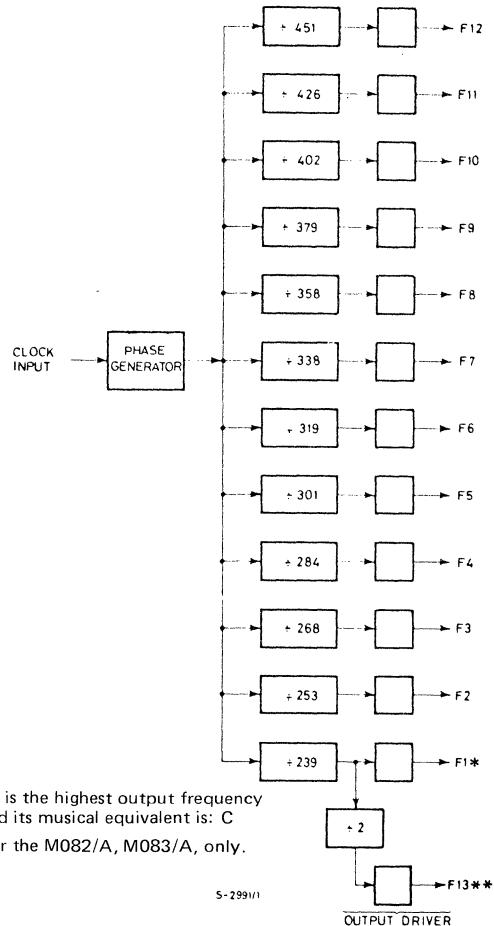
PIN CONNECTIONS



* V_{DD} is the highest supply voltage

** V_{SS} is the lowest supply voltage

BLOCK DIAGRAM



* F1 is the highest output frequency
and its musical equivalent is: C

** For the M082/A, M083/A, only.

RECOMMENDED OPERATING CONDITIONS

Parameter	Test conditions	Values			Unit
		Min.	Typ.	Max.	
V_{SS}	Lowest supply voltage	0		0	V
V_{DD}	Highest supply voltage	+10	+12	+14	V

ELECTRICAL CHARACTERISTICS ($0^{\circ}\text{C} \leq T_{\text{amb}} \leq 50^{\circ}\text{C}$; $V_{\text{SS}} = 0\text{V}$; $V_{\text{DD}} = +10\text{V}$ to $+14\text{V}$ unless otherwise specified)

Parameter	Test conditions	Values			Unit	Fig.
		Min.	Typ.	Max.		
V_{IL}	Input clock, low		V_{SS}	$V_{\text{SS}}+1$	V	1
V_{IH}	Input clock, high		$V_{\text{DD}}-1$	V_{DD}	V	
t_r, t_f	Input clock rise and fall times 10% to 90%	4.5 MHz		30	ns	1
t_{on}, t_{off}	Input clock on and off times	4.5 MHz		111	ns	1
C_I	Input capacitance			5	10	pF
V_{OH}	Output high	0.75 mA	$V_{\text{DD}}-1.5$	V_{DD}	V	2
V_{OL}	Output low	0.70 mA	V_{SS}	$V_{\text{SS}}+1$	V	2
t_{ro}, t_{fo}	Output rise and fall times 500 pF load		250	2500	ns	3
t_{on}, t_{off}	Output duty cycle	M 082		30		
		M 083, M 086		50	%	
I_{DD}	Supply current			24	35	mA
f_I	Input clock frequency	M 082, M 083, M 086	100	4000.48	4500	kHz
f_I	Input clock frequency	M 082A, M 083A, M 086A	100	2000.24	2500	kHz

* Output unloaded.

Fig. 1 Input clock waveform

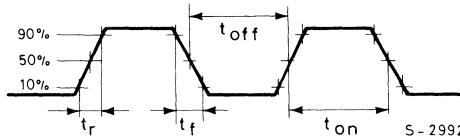
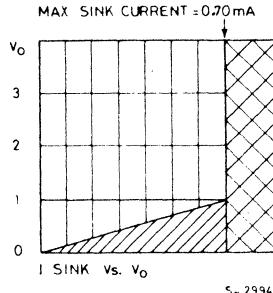
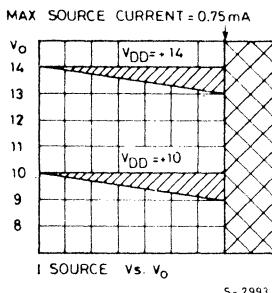


Fig. 2 – Output signal d.c. loading



(OPERATING AREA)

(CURRENT OVERLOAD AREA)

SS

M 082/A
M 083/A
M 086/A

Fig. 3 – Output loading

