BUS SIGNAL USAGE FOR ALL IMSAI PRODUCTS

REVISION HISTORY

1.0	09-Mar-2021	First release. Missing EXP-10, PROG-8, RAM-16, RAM-32, RAM-65
1.1	20-Mar-2021	Added EXP-10 signals.
1.2	22-Jun-2021	Added RAM-16 signals. Grouped board sets such as IFM/FIB.

Legend	Meaning
O	Output: Driven by board
I	Input: Received by board
3S	Three-state driven by board
OC	Open-collector driven by board
(B)	Backplane signal
(S)	Driven by slave boards
(M)	Driven by master boards
(M/S)	Driven by master and slave boards
LED+	Signal sources current to LED
LED-	Signal sinks current through LED
↑	Rising edge
↓	Falling edge
→	Connects to
↔	Jumper option
DS	DIP switch
T	True (electrical level depends on signal specification)
F	False (electrical level depends on signal specification)
PU	Pull-up resistor

IMSAI Product S-100 Bus Signal Usage

IMSAI NAME	+8V	+16V	XRDY	/VI0 - /VI7	XRDY2	AA14	AA15	A18	A16	A17	/STSDSBL	/CCDSBL	UNPROT
IEEE 696 NAME	+8 V	+16 V	XRDY	VI0* - VI7*	NMI*	PWRFAIL*	DMA3*	A18	A16	A17	SDSB*	CDSB*	GND
IEEE 696 USE	B	B	S	S	S	B	M	M	M	M	M	M	
S-100 PIN	1 51	2	3	4-11	12	13	14	15	16	17	18	19	20
CP-A	X		O										→ T5. **Probably ill-advised.**
DIO	X					I ↔	I ↔	I	I, OC ↔ phantom	I			
PDS	X	X											
PDS II	X	X											
EXP-10				O (VI7 only, **violates spec**)									
IFM	X	X									OC	OC	
FIB	X			OC ↔									
MIO	X	X		OC ↔									
MPU-A	X	X	I, PU								I, PU	I, PU	
MPU-B	X	X		OC ↔	I, PU						I, PU	I, PU	
PIC-8	X			I									
PIO 4	X			OC ↔									
PIO 6	X	X		OC ↔									
PROG-8													
PROM-4	X												
RAM 4A	X			OC ↔									I, ↔ GND.
RAM-16/32/65	X	X				I ↔	I ↔	I	I	I	I		
RAM-III	X	X				I ↔	I ↔	I	I	I	I		
SIO	X	X		OC ↔									
VIO	X	X				I ↔	I ↔	I	I, OC ↔ phantom	I			

IMSAI Product S-100 Bus Signal Usage

IMSAI NAME	/DIDSBL	/ADDR DSBL	/DODSBL	Φ2	Φ1	PHLDA	PWAIT	PINTE	A0 - A15	DO0 - DO7	DI0 - DI7
IEEE 696 NAME	RFU	ADSB*	DODSB*	Φ	pSTVAL*	pHLDA	RFU	RFU	A0 - A15	DO0 - DO7	DI0 - DI7
IEEE 696 USE		M	M	B	M	M			M	M	M
S-100 PIN	21	22	23	24	25	26	27	28	29-34 37 79-87	35 36 38-40 88-90	41-43 91-95
CP-A	O: Force local data bus to CPU.			I ↓ RUN sync. ↑ Detects M1 state (see notes).		LED+	LED+	LED+	LED+	I: DO5 only (see notes).	
DIO									I ↔ A14, A15	I	3S
PDS											
PDS II											
EXP-10											
IFM		OC	OC	↓ Advances state machine.		I	3S	OC	3S	3S	I
FIB											
MIO				Baud rate clock. **Should use /CLK (49).**					I A0-A7	I	3S
MPU-A	I, PU	I, PU	I,PU	O	O	3S	3S	3S	3S	3S	I
MPU-B	I, PU	I, PU	I,PU	O	O	3S	3S	PU ↔	3S	3S	I
PIC-8				I (see notes).				I	I A0-A7	I	3S (DI3, DI4, DI5 only)
PIO 4									I		
PIO 6				I					I		
PROG-8											
PROM-4				I (see notes).					I		3S
RAM 4A							I		I	I	3S
RAM-16/32/65				I	I: See PSYNC (25)				I ↔ A14-A15	I	3S
RAM-III					I: See PSYNC (25)		I		I ↔ A12-A15	I	3S
SIO				Baud rate clock. **Should use /CLK (49).**					I	I	3S
VIO				↑ wait clock.	I: See PSYNC (25)		I		I ↔ A14, A15	I	3S

IMSAI Product S-100 Bus Signal Usage

IMSAI NAME	SM1	SOUT	SINP	SMEMR	SHLTA	/CLK	GND	−16V	/SSW DSB	/EXT CLR	CH GND		
IEEE 696 NAME	sM1	sOUT	sINP	sMEMR	sHLTA	CLOCK	GND	−16 V	GND	SLAVE CLR*	DMA0*	DMA1*	DMA2*
IEEE 696 USE	M	M	M	M	M	B	B	B		B	M	M	M
S-100 PIN	44	45	46	47	48	49	50 100	52	53	54	55	56	57
CP-A	LED+	I, LED+	I, LED+	LED+	LED+		X		O: Force local data bus to S-100 bus. **IEEE 696 Conflict.**	OC: pRESET + EXT CLEAR switch			
DIO		I	I	I		I	X			I			
PDS							X						
PDS II							X	X					
EXP-10					I **(violates spec)**								
IFM		I, 3S	OC	3S			X	X					
FIB							X						
MIO		I	I				X	X		I			
MPU-A	3S	3S	3S	3S	3S	O	X	X	I				
MPU-B	3S	3S	3S	3S	3S	O	X	X		OC, PU			
PIC-8		I					X						
PIO 4		I	I				X			I			
PIO 6		I	I	I			X	X		I			
PROG-8													
PROM-4				I			X	X					
RAM 4A		I	I	I			X			I			
RAM-16/32/65	I	I	I	I	I		X	X					
RAM-III	I			I	I		X	X					
SIO		I	I				X	X		I			
VIO		I	I				X	X					

IMSAI Product S-100 Bus Signal Usage

IMSAI NAME					AA13	AA12	A19	MWRITE	/PS	PROT	RUN	PRDY	/PINT	/PHOLD
IEEE 696 NAME	sXTRQ*	A19	SIXTN*	A20 - A23	NDEF	NDEF	PHANTOM*	MWRT	RFU	GND	NDEF	RDY	INT*	HOLD*
IEEE 696 USE	M	M	S	M			M/S	B				S	S	M
S-100 PIN	58	59	60	61-64	65	66	67	68	69	70	71	72	73	74
CP-A								O		→ GND	O			
DIO							I					OC		
PDS														
PDS II														
EXP-10														
IFM							OC (/REF DSBL)					I		I, OC
FIB														
MIO													↔ /VI0 (4).	
MPU-A											I: PU	I, PU	I, PU	I
MPU-B								O: ↔ DS			I: PU	I, PU	I, PU ↔ /VI7.	I, PU
PIC-8													O	
PIO 4								I						
PIO 6								I				3S	OC ↔	
PROG-8														
PROM-4												3S		
RAM 4A								I	3S	I		3S	OC ↔	
RAM-16/32/65							I	I	I ↔		I	3S		
RAM-III					I ↔	I ↔	I	I	I ↔		I	OC		
SIO								I						
VIO							I					OC		

IMSAI Product S-100 Bus Signal Usage

IMSAI NAME	/PRESET	PSYNC	/PWR	PDBIN	SINTA	/SWO	SSTACK	/POC	
IEEE 696 NAME	RESET*	pSYNC	pWR*	pDBIN	sINTA	sWO*	ERROR*	POC*	
IEEE 696 USE	B	M	M	M	M	M	S	B	
S-100 PIN	75	76	77	78	96	97	98	99	I/O Addressing
CP-A	OC: RESET switch	I: T detects M1 state (see notes). ↑ advances instruction state machine. ↓ resets switch FFs.	I	I	LED+	LED+	LED+	I	Upper 8 bits
DIO			I	I	I			I	Lower 8 bits
PDS									
PDS II									
EXP-10				I	I				
IFM	I: 0.1µF to GND.	OC (This may be why VIO claims it cannot be written by DMA)	I, 3S	3S	OC	3S			
FIB									
MIO			I	I				I	Lower 8 bits
MPU-A	I: 33µF to GND.	3S	3S	3S	3S	3S	3S	O	
MPU-B	I: 4.7µF to GND.	3S	3S	3S	3S	3S	↔ GND.	OC	Upper 8 bits
PIC-8			I		I				Lower 8 bits
PIO 4			I	I					Lower 8 bits
PIO 6		I	I	I	I				Lower 8 bits
PROG-8									
PROM-4		I (see notes).							
RAM 4A			I	I					
RAM-16/32/65	OC: Power-up	I: ↑ or ↓ (PSYNC • Φ1) address latch ↔.	I	I	I			I	
RAM-III		I: ↑ or ↓ (PSYNC • Φ1) address latch ↔.	I	I				I	
SIO			I	I				I	Lower 8 bits
VIO		I: ↑ or ↓ (PSYNC • Φ1) address latch ↔.	I	I	I			I	

IMSAI NAME	
IEEE 696 NAME	
IEEE 696 USE	
S-100 PIN	**Notes**
CP-A	STOP on M1 cycle uses pSYNC • -Φ2 • DO5. Very 8080-specific.
DIO	Memory address hardwired to Exxx.
PDS	
PDS II	
EXP-10	
IFM	
FIB	
MIO	
MPU-A	
MPU-B	
PIC-8	Output port decode: ADDR.EQ • Φ2 • -PWR* • SOUT
PIO 4	May be configured for memory map at FFxx.
PIO 6	
PROG-8	
PROM-4	Wait state counts ↓ Φ2 when PSYNC = F.
RAM 4A	
RAM-16/32/65	
RAM-III	
SIO	May be configured for memory map at FExx.
VIO	