PROPOSED STANDARD FOR THE S-100 BUS

Preliminary Specification, IEEE Task 696.1/D2

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The computer bus commonly known as the S-100 was first introduced by MITS, Inc., with its Altair kit. This bus has since spread throughout the electronics industry and beyond. Today over a hundred manufacturers make products which claim to be compatible with the S-100 bus even though—until now—no complete specification has been available. The following table, figures, and notes constitute the preliminary draft of a proposed standard for the S-100 bus.

This document is a specification for both timing and signal disciplines. Signal discipline is described using the bus master/bus slave language long associated with Digital Equipment Corporation's PDP-11. This point of view facilitated the development of a simple and highly reliable DMA protocol, the extended addressing capabilities, and the 16-bit wide data path proposals. These extensions to the original Altair bus represent a significant advance to the state of the art of small computers and are a direct result of a continuing dialogue with a large number of interested people who have contributed their thoughts and ideas to the standards committee. The extended address and data proposals are compatible with systems that don't use these features, including most existing systems. Signals which are defined or redefined for the extensions are indicated by an asterisk.

The preliminary specification will be presented at the 1978 NCC in June in Anaheim, California. Comments can be made at that time or by writing to George Morrow,

S-100 Bus Signal Definitions (preliminary—subject to revision)

PIN NO.	SIGNAL NAME & TYPE	POLARITY	DESCRIPTION
1	+8 volts (B)[1]		Instantaneous minimum greater than 7 volts, instantaneous maximum less than 25 volts, average maximum less than 11 volts.
2	+16 volts (B)		Instantaneous minimum greater than 14 volts, instantaneous maximum less than 35 volts, average maximum less than 20 volts.
3	XRDY (S)[1,10]	positive	One of two ready inputs to the current bus master. The bus is ready when both these ready inputs are true.
4	VI0 (S)[10]	negative	Vectored interrupt line 0.
5	VI1 (S)[10]	negative	Vectored interrupt line 1.
6	VI2 (S)[10]	negative	Vectored interrupt line 2.
7	VI3 (S)[10]	negative	Vectored interrupt line 3.
8	VI4 (S)[10]	negative	Vectored interrupt line 4.
9	VI5 (S)[10]	negative	Vectored interrupt line 5.
10	VI6 (S)[10]	negative	Vectored interrupt line 6.
11	VI7 (S)[10]	negative	Vectored interrupt line 7.
12	—	—	Not specified.
13	—	—	Not specified.
14	—	—	Not specified.
15	—	—	Not specified.
16	—	—	Not specified.
17	—	—	Not specified.
18	$\overline{\text{STAT DSB}}$ (M)[1,10]	negative	The control signal to disable the 9* status signals.[2]
19	$\overline{\text{C/C DSB}}$ (M)[10]	negative	The control signal to disable the 6 command/control signals.[3]
20	UNPROT	—	Not specified.
21	SS	—	Not specified.
22	$\overline{\text{ADD DSB}}$ (M)[10]	negative	The control signal to disable the 16 address signals.[4]

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S-100 Bus Signal Definitions (preliminary—subject to revision)

PIN NO.	SIGNAL NAME & TYPE	POLARITY	DESCRIPTION
23	$\overline{\text{DO DSB}}$ (M)[10]	negative	The control signal to disable the 8 data output signals.[8]
24	ϕ_2 (B)	positive	The master timing signal for the bus.
25	ϕ_1	—	Not specified.
26	PHLDA (M)	positive	A command/control signal used in conjunction with PHOLD to coordinate bus master transfer operations.
27	PWAIT (M)	positive	The acknowledge signal to either of the bus ready signals XRDY, PRDY or to a HLT instruction.
28	PINTE	positive	Not specified.
29	A5 (M)	positive	Address bit 5.
30	A4 (M)	positive	Address bit 4.
31	A3 (M)	positive	Address bit 3.
32	A15 (M)	positive	Address bit 15 (most significant for non-extended addressing).
33	A12 (M)	positive	Address bit 12.
34	A9 (M)	positive	Address bit 9.
*35	DO1 (M)/A17 (M)/DATA1 (M/S)[11,12]	positive	Data out bit 1, extended address bit 17, bidirectional data bit 1.
*36	DO0 (M)/A16 (M)/DATA0 (M/S)	positive	Data out bit 0, extended address bit 16, bidirectional data bit 0 (least significant).
37	A10 (M)	positive	Address bit 10.
*38	DO4 (M)/A20 (M)/DATA4 (M/S)	positive	Data out bit 4, extended address bit 20, bidirectional data bit 4.
*39	DO5 (M)/A21 (M)/DATA5 (M/S)	positive	Data out bit 5, extended address bit 21, bidirectional data bit 5.
*40	DO6 (M)/A22 (M)/DATA6 (M/S)	positive	Data out bit 6, extended address bit 22, bidirectional data bit 6.
*41	DI2 (M)/DATA10(M/S)[6]	positive	Data in bit 2, bidirectional data bit 10.
*42	DI3 (M)/DATA11 (M/S)	positive	Data in bit 3, bidirectional data bit 11.
*43	DI7 (M)/DATA15 (M/S)	positive	Data in bit 7, bidirectional data bit 15 (most significant).
44	SM1 (M)	positive	The status signal which indicates that the current cycle[7] is an op-code fetch.
45	SOUT (M)	positive	The status signal identifying the data transfer bus cycle of an OUT instruction.
46	SINP (M)	positive	The status signal identifying the data transfer bus cycle of an IN instruction.
47	SMEMR (M)	positive	The status signal identifying bus cycles which transfer data from memory to a bus master which are not interrupt acknowledge instruction fetch cycle(s).
48	SHLTA (M)	positive	The status signal which acknowledges that a HLT instruction has been executed.

Cont'd on overleaf

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The committee is currently considering proposals for DMA and interrupt priority specifications. These will be made public in the near future—perhaps at the NCC meeting.

Bus signal notes (see table)

1. There are three types of signals on the S-100 bus. M stands for bus master. Signals designated by (M) are those which a bus master must generate. The bus master currently controlling the bus has the responsibility for faithfully generating *all* signals of type M during its control of the bus.

S stands for bus slave. A bus slave need generate only that subset of type S signals which are necessary to communicate with bus masters which have the ability to address the slave.

B stands for bus. Any bus signal which is not of type M or S is by default type B. This is not to say that some bus master is not in fact generating one or more type B signals. Rather a type B signal is one that (a) not all bus masters are required to generate, and (b) not any bus slave is required to generate.

A bus master is, by definition, a bus device which generates at least all of the type M signals. A bus slave is a bus device which generates some subset of type S signals. A bus master may also be a bus slave and vice-versa. Memory devices are almost always bus slaves while DMA devices are usually both a bus master (data transfers) and a bus slave (accepting commands). Central processing units are usually bus masters.

2. The 9* status signals are SMEMR, SINP, SM1, SOUT, SHLTA, SSTACK (not specified), $\overline{\text{SWO}}$, SINTA, and SXTRQ.

3. The 6 command/control signals are PHLDA, PSYNC, PDBIN, PINTE (not specified), $\overline{\text{PWR}}$, and PWAIT.

4. The 16 address signals are A15, A14, A13, A12, A11, A10, A9, A8, A7, A6, A5, A4, A3, A2, A1, and A0.

5. Data output is specified relative to a bus master. By definition, data which is transmitted by a bus

master is always data output and occurs on the DO bus or DATA* bus.

6. Data input is specified relative to a bus master. By definition, data which is received by a bus master is always data input and occurs on the DI bus or DATA* bus.

7. A bus cycle is a collection of bus states (BS_α). A bus cycle always starts with a BS_1 state which is followed by a BS_2 state. After BS_2 comes an indeterminate number of BS_w (bus wait) states. A bus cycle may have zero BS_w states or it may have an arbitrarily large number of BS_w states. BS_3 is the bus state which follows BS_w (or BS_2 if there are no BS_w states present). BS_3 is followed by zero or more BS_i (bus idle) states. A BS_3 or BS_i state terminates a bus cycle.

8. The DO bus is the following set of signals: DO7, DO6, DO5, DO4, DO3, DO2, DO1, and DO0.

9. The DI bus is the following set of signals: DI7, DI6, DI5, DI4, DI3, DI2, DI1, and DI0.

10. These signals should be generated by an open collector bus driver capable of sinking at least 24 mA at no more than 0.5 volts.

*11. During the last half of bus state 1 and the first half of bus state 2, the DO lines are used to furnish extended addressing to slaves that can utilize this information.

*12. For 16-bit masters and slaves, the DI and DO lines gang together to form a 16-bit bidirectional data bus called DATA0-15. The DO lines carry the low-order byte while the DI lines accommodate the high-order byte. The configuration of the DI and DO buses is governed by the signals $\overline{SXTRQ}$ and $\overline{SIXTN}$. When both these signals are low, the DI and DO lines become bidirectional. Otherwise, DI carries the data to the current master while DO carries data to the addressed slave.

Signal characteristics

Bus drivers must sink at least 24 mA at no more than 0.5 volts. Except for open collector drivers, they must source at least 2 mA at no less than 2.4 volts.

Bus receivers must have diode clamps to prevent excessive negative excursions. Any bus signal less than 0.8 volts must be recognized as a logic zero, and any signal more than 2 volts must be interpreted as a logic one.

Receivers are to source no more than 0.8 mA at 0.5 volts and are to sink no more than 80 μA at 2.4 volts. The capacitance load of an input from the bus must not exceed 25 pF.

S-100 Bus Signal Definitions (preliminary—subject to revision)

PIN NO.	SIGNAL NAME & TYPE	POLARITY	DESCRIPTION
49	$\overline{CLOCK}$ (B)	—	2 MHz, 40-60% duty cycle. Not required to be synchronous with any other bus signals.
50	GND		Signal and power ground.
51	+8 volts (B)		See comments for pin number 1.
52	−16 volts (B)		Instantaneous maximum less than −14 volts, instantaneous minimum greater than −35 volts, average minimum greater than −20 volts.
53	$\overline{SSWI}$	—	Not specified.
54	$\overline{EXT\ CLR}$	negative	A reset signal to rest bus slaves. When this signal goes low, it must stay low for at least 3 bus states.
55	—	—	Not specified.
56	—	—	Not specified.
57	—	—	Not specified.
58	—	—	Not specified.
*59	$\overline{SXTRQ}$ (M)	negative	The status signal which requests 16-bit wide slaves to respond by asserting $\overline{SIXTN}$.
60	—	—	Not specified.
*61	$\overline{SIXTN}$ (S)	negative	The signal generated by 16-bit slaves in response to the 16-bit request status signal SXTRQ.
62	—	—	Not specified.
63	—	—	Not specified.
64	—	—	Not specified.
65	—	—	Not specified.
66	—	—	Not specified.
67	$\overline{PHANTOM}$ (B)	negative	A bus signal which disables normal slave devices and enables phantom slaves—primarily used for bootstrapping systems without hardware front panels.
68	MWRITE (B)	positive	MWRITE = $\overline{(PWR)}$ • SOUT. This signal must follow PWR by not more than 30 ns.
69	$\overline{PS}$	—	Not specified.
70	PROT	—	Not specified.
71	RUN	—	Not specified.
72	PRDY (S)[10]	positive	See comments for pin number 3.
73	$\overline{PINT}$ (S)[10]	negative	The primary interrupt request bus signal.
74	$\overline{PHOLD}$ (M)[10]	negative	The command/control signal used in conjunction with PHLDA to coordinate bus master transfer operations.
75	$\overline{PRESET}$ (B)[10]	negative	The reset signal to reset bus master devices. When this signal goes low, it must stay low for at least 3 bus states.

S-100 Bus Signal Definitions (preliminary—subject to revision)

PIN NO.	SIGNAL NAME & TYPE	POLARITY	DESCRIPTION
76	PSYNC (M)	positive	The command/control signal identifying BS_1. (See bus state comments.)
77	$\overline{PWR}$ (M)	negative	The command/control signal signifying the presence of valid data on DO bus[8] or DATA* bus.[12]
78	PDBIN (M)	positive	The command/control signal that requests data on the DI bus[9] or DATA* bus[12] from the currently addressed slave.
79	A0 (M)	positive	Address bit 0 (least significant).
80	A1 (M)	positive	Address bit 1.
81	A2 (M)	positive	Address bit 2.
82	A6 (M)	positive	Address bit 6.
83	A7 (M)	positive	Address bit 7.
84	A8 (M)	positive	Address bit 8.
85	A13 (M)	positive	Address bit 13.
86	A14 (M)	positive	Address bit 14.
87	A11 (M)	positive	Address bit 11.
*88	DO2 (M)/A18 (M)/DATA2 (M/S)	positive	Data out bit 2, extended address bit 18, and bidirectional data bit 2.
*89	DO3 (M)/A19 (M)/DATA3 (M/S)	positive	Data out bit 3, extended address bit 19, and bidirectional data bit 3.
*90	DO7 (M)/A23 (M)/DATA7 (M/S)	positive	Data out bit 7 (most significant for 8-bit data), extended address bit 23, and bidirectional data bit 7.
*91	DI4 (S)/DATA12 (M/S)	positive	Data in bit 4 and bidirectional data bit 12.
*92	DI5 (S)/DATA13 (M/s)	positive	Data in bit 5 and bidirectional data bit 13.
*93	DI6 (S)/DATA14 (M/S)	positive	Data in bit 6 and bidirectional data bit 14.
*94	DI1 (S)/DATA9 (M/S)	positive	Data in bit 1 and bidirectional data bit 9.
*95	DI0 (S)/DATA8 (M/S)	positive	Data in bit 0 (least significant for 8-bit data) and bidirectional data bit 8.
96	SINTA (M)	positive	The status signal identifying the instruction fetch cycle(s) that immediately follow an accepted interrupt request presented on PINT.
97	$\overline{SWO}$ (M)	negative	The status signal identifying a bus cycle which transfers data from a bus master to a slave.
98	SSTACK	—	Not specified.
99	$\overline{POC}$ (B)	negative	The power-on clear signal for all bus devices; when this signal goes low, it must stay low for at least 3 bus states.
100	GND		Signal and power ground.

Bus state comments

BS_1 is the initial bus state of a bus cycle. The address lines, data and status, are in a state of flux during most of BS_1, and PSYNC is active starting with the second half of BS_1.

BS_2 is the second bus state when address data, status, and ready signals become stable.

BS_w states occur as needed to synchronize a bus master with a bus slave which has brought one of the ready lines false.

BS_3 is the data transfer state when a bus master transfers data to a slave or vice-versa.

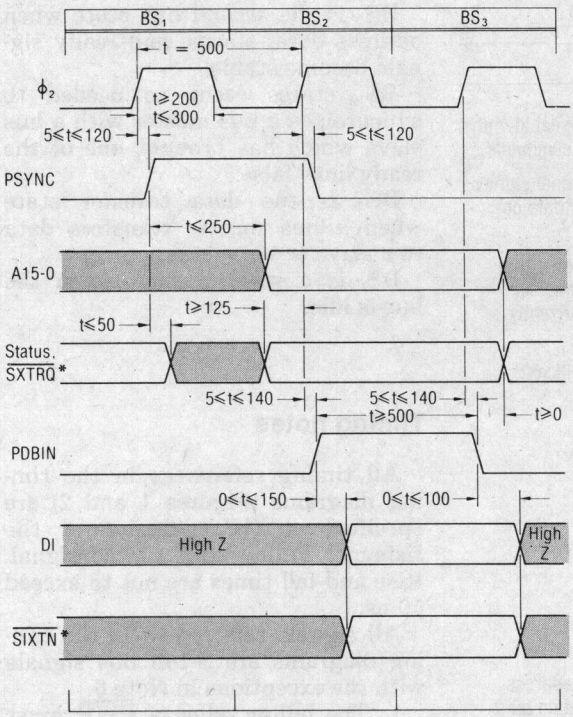
BS_i is a state during which the bus is idle.

Timing notes

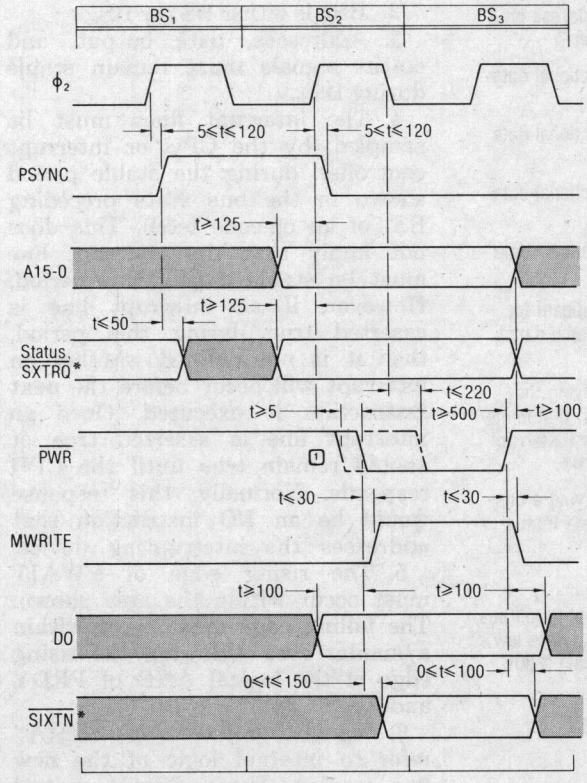
All timing references in the timing diagrams (Figures 1 and 2) are specified at the midpoint of the rising or falling edge of the signal. Rise and fall times are not to exceed 50 ns.

All signals referred to in the timing diagrams are S-100 bus signals with the exceptions in Note 6.

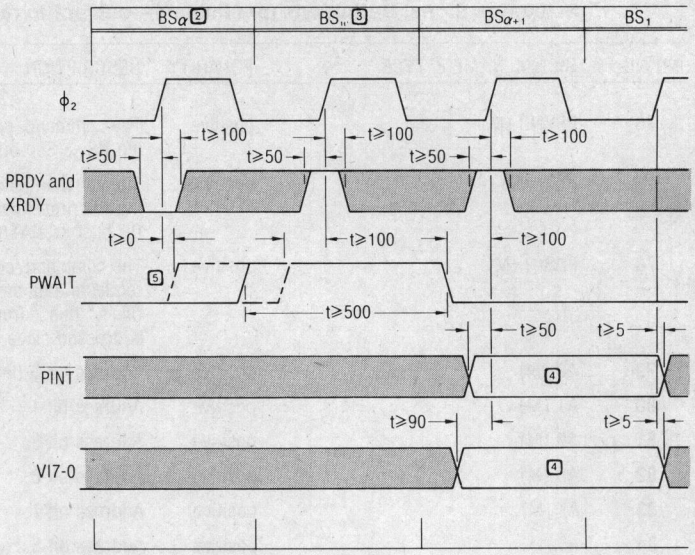
1. The falling edge of $\overline{PWR}$ must occur within the area shown. The rising edge must occur within a similar area of the next bus state.
2. BS_α is either BS_2 or BS_w.
3. Addresses, data output, and status signals must remain stable during BS_w.
4. The interrupt lines must be sampled, by the CPU or interrupt controller, during the stable period shown in the bus state preceding BS_1 of an op-code fetch. This does not imply that the interrupt line must be stable during this period. However, if an interrupt line is asserted true during this period, then it is not defined whether an interrupt will occur before the next instruction is executed. Once an interrupt line is asserted true, it should remain true until the CPU responds. Normally, this response would be an I/O instruction that addresses the interrupting device.
5. The rising edge of PWAIT must occur within the area shown. The falling edge must occur within a similar area following the rising edge of the logical AND of PRDY and XRDY.
6. Signals prefixed by "DMA" refer to internal logic of the new bus master. These signals control the buffers of this bus master which drive the command and control, status, address, and data output bus lines. The timing diagram depicts logic levels which are high when these buffers are disabled.



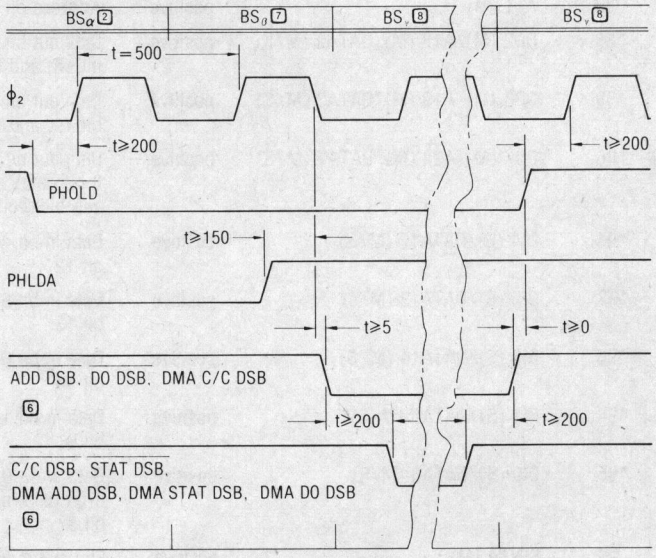
(a) Memory or I/O read.



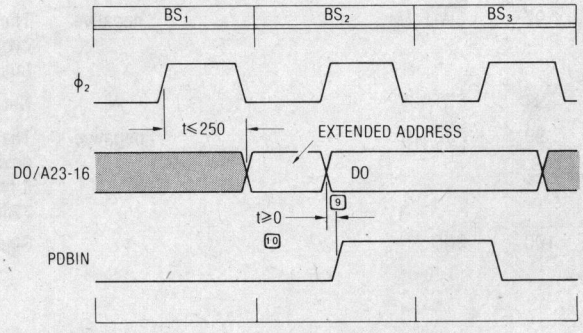
(b) Memory or I/O write.



(c) Interrupt and wait timing.



(d) Bus exchange timing.



*(e) Extended addressing.

Figure 1. S-100 bus timing, in nanoseconds, for (a) memory or I/O read, (b) memory or I/O write, (c) interrupt and wait, (d) bus exchange, and *(e) extended addressing (preliminary—subject to revision).

7. BS_β is either BS_3 or BS_i.

8. BS_γ is either BS_i or BS_1.

*9. Extended address bits A16 through A23 are multiplexed on the DO lines. They must occur as shown within 250 ns after the rising edge of ϕ_2 during BS_1. During a write, data must appear on these lines 100 ns before $\overline{PWR}$ is active. The $\overline{PWR}$ signal can be asserted as soon as 5 ns after the rising edge of ϕ_2 during BS_2. Therefore, under worst case conditions, the extended addresses are on the bus for 155 ns. Masters can generate $\overline{PWR}$ later as shown. This would allow the extended addresses to be on the bus longer. However, slaves should be designed to correctly respond in the worst case situation.

*10. To avoid conflict on the DO lines during a 16-bit read, similar to the situation described in Note 9 above, the extended addresses must be removed from the DO lines before the rising edge of PDBIN.

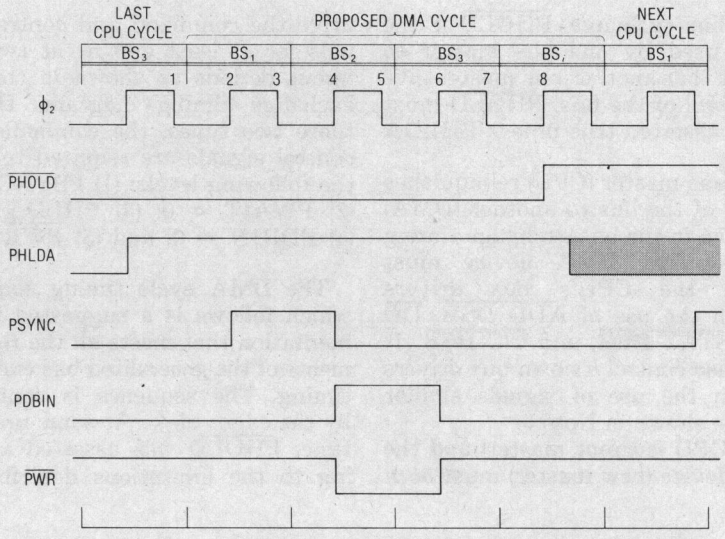


Figure 2. Proposed DMA protocol (preliminary—subject to revision).

Direct memory access requirements

A DMA cycle is a special case of a bus master taking over the bus to execute a memory read or write cycle. A DMA device is required to generate *all* type M (bus master) signals on the bus, and control the bus exchange.

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Microprocessor Standards Discussed

Proposed standards for instruction sets, relocatable software, floating point arithmetic, and buses were considered in an open meeting of the IEEE Computer Society's Microprocessor Standards Committee, chaired by Robert G. Stewart.[1] The meeting, held during Compcon Spring, attracted an audience of about 30 people. The committee hopes to complete most of the IEEE standards approval process by the end of the year.

The second draft of the Standard for Microprocessor Instructions and Assemblers, presented by Wayne Fischer, proposed uniform requirements for instruction names and mnemonics, operand syntax, and comments, as well as rules for generating new mnemonics. The need for this standard is revealed by the fact that the several manufacturers of 8080-like microprocessors now use different mnemonics for semantically identical instructions. Standardization of this area will make it easier for users to learn another microprocessor and to transport assembler programs.

Tom Pittman identified several aspects of the relocatable software format task. Software for 8080-like microprocessors such as the 8080A, 8085, and Z-80 could have moveable object code. Different operating systems assume memory to be in different places. Object modules from new, higher-order languages should run under the "old" operating systems. Object modules should be combined by a linker rather than by re-assembly.

Based on a sample of six formats, Pittman found that presently available formats seem to be language dependent and have insufficient flexibility. There seems to be an implied "standard" linker for which the choices are to build on an existing format or define a new one. However, there seems to be no one, suitable existing format and willingness to define a new format is lacking so far on the part of some major microprocessor manufacturers, at least on an industry basis.

The base material for the floating point task was a proposal from Intel.[2] Dick Delp identified the key factors as tradeoff between speed and mathematical rigor, processor independence of format, and level of implementation. The committee resolved most issues, microprocessor independence, for example, in favor of rigor.

The microprocessor bus task includes two board-level buses, the Intel Multibus and the S-100 bus, and a component level bus, the Microbus from National Semiconductor.

George Morrow pointed out that products for the S-100 bus now being supplied by some 150 vendors are not really compatible. The current work is primarily to specify existing practice using master/slave concepts. New ground in the form of a DMA protocol has been broken.

Extending the S-100 bus to 24 address bits and 16 data bits was recommended by Dave Gustavson. Exactly how this will be done is presently under consideration.

The component-level Microbus is intended to be processor independent and to be used by systems of less than ten integrated circuits, according to Gordon Force. The specification, in work since last summer, will emphasize AC timing characteristics.

Drafts of proposed standards will be available by writing to the committee chairman, Robert G. Stewart, 1658 Belvair Drive, Los Altos, CA 94022. Some drafts will be published in *Computer* as they near final form. ■

References

1. Robert G. Stewart, "Standards For Microprocessors," *Computer*, Vol. 11, No. 3, March 1978, pp. 65-66.

2. John F. Palmer, "The Intel Standard For Floating-Point Arithmetic," *Proc. Compsac 77*, pp. 107-112.

The bus exchange. $\overline{\text{PHOLD}}$ is the signal used by one bus master to request that another bus master give up control of the bus. $\overline{\text{PHOLD}}$ must not be asserted true unless PHLDA is false.

One bus master (CPU) relinquishes control of the bus to another (DMA) as shown in the bus exchange timing diagram. The DMA device must control the CPU's bus drivers through the use of $\overline{\text{ADD DSB}}$, $\overline{\text{DO DSB}}$, $\overline{\text{STAT DSB}}$, and $\overline{\text{C/C DSB}}$. It must also control its own bus drivers through the use of signals similar to those shown in Note 6.

The CPU (current master) and the DMA device (new master) must *both* drive the command and control signals for at least 200 ns at two different periods as shown in the bus exchange timing diagram. During these two times, the command and control signals are required to have the following levels: (1) PSYNC = 0; (2) PWAIT = 0; (3) PHLDA = 1; (4) PDBIN = 0; and (5) $\overline{\text{PWR}}$ = 1.

The DMA cycle timing sequence which follows is a suggested implementation that meets all the requirements of the generalized bus exchange timing. The sequence is controlled by the edges of ϕ_2. At some previous time, $\overline{\text{PHOLD}}$ was asserted according to the limitations described in the first paragraph of this section. PHLDA is asserted true by the CPU during BS_3 of the last CPU bus cycle. The bus exchange begins on the falling edge of ϕ_2 while PHLDA is true (labeled 1 on the timing diagram). The DMA bus cycle then proceeds as described in the following section. At edge 8 of ϕ_2 $\overline{\text{PHOLD}}$ is driven false by the DMA device and henceforth the CPU is again in control of the bus.

Proposed DMA cycle sequence.

ϕ_2 edge:

1. CPU address and data bus drivers turned off. DMA command and control drivers turned on. The CPU and DMA command and control signals must match the levels described in the previous section.
2. CPU status and command and control drivers turned off. DMA address, data output, and status drivers turned on. PSYNC = 1.
3. No change.
4. PSYNC = 0. PDBIN = 1 if memory read or $\overline{\text{PWR}}$ = 0 if memory write.
5. No change.
6. PDBIN = 0 and $\overline{\text{PWR}}$ = 1.
7. CPU command and control drivers turned on. DMA address and data output drivers turned off.
8. CPU address, data output, and status drivers turned on. DMA status and command and control drivers turned off. $\overline{\text{PHOLD}}$ =1.

Multiple data transfers can occur by repeating steps 2 through 6. ■

Acknowledgment

We would like to thank the other members of the Microprocessor Standards Committee for their support and invaluable comments. Special thanks to Robert Stewart who is chairman of the committee. His leadership and organizational skills have been a great aid to all of us.

We would also like to extend our thanks to Kells Elmquist and Steve Edleman of Ithaca Audio. Both of these gentlemen flew out to the Second Computer Faire to discuss their ideas about S-100 bus extensions with us. Several of their ideas were truly inspirational. Their intellectual prodding was the force which created the extended addressing and the bidirectional data bus proposals.