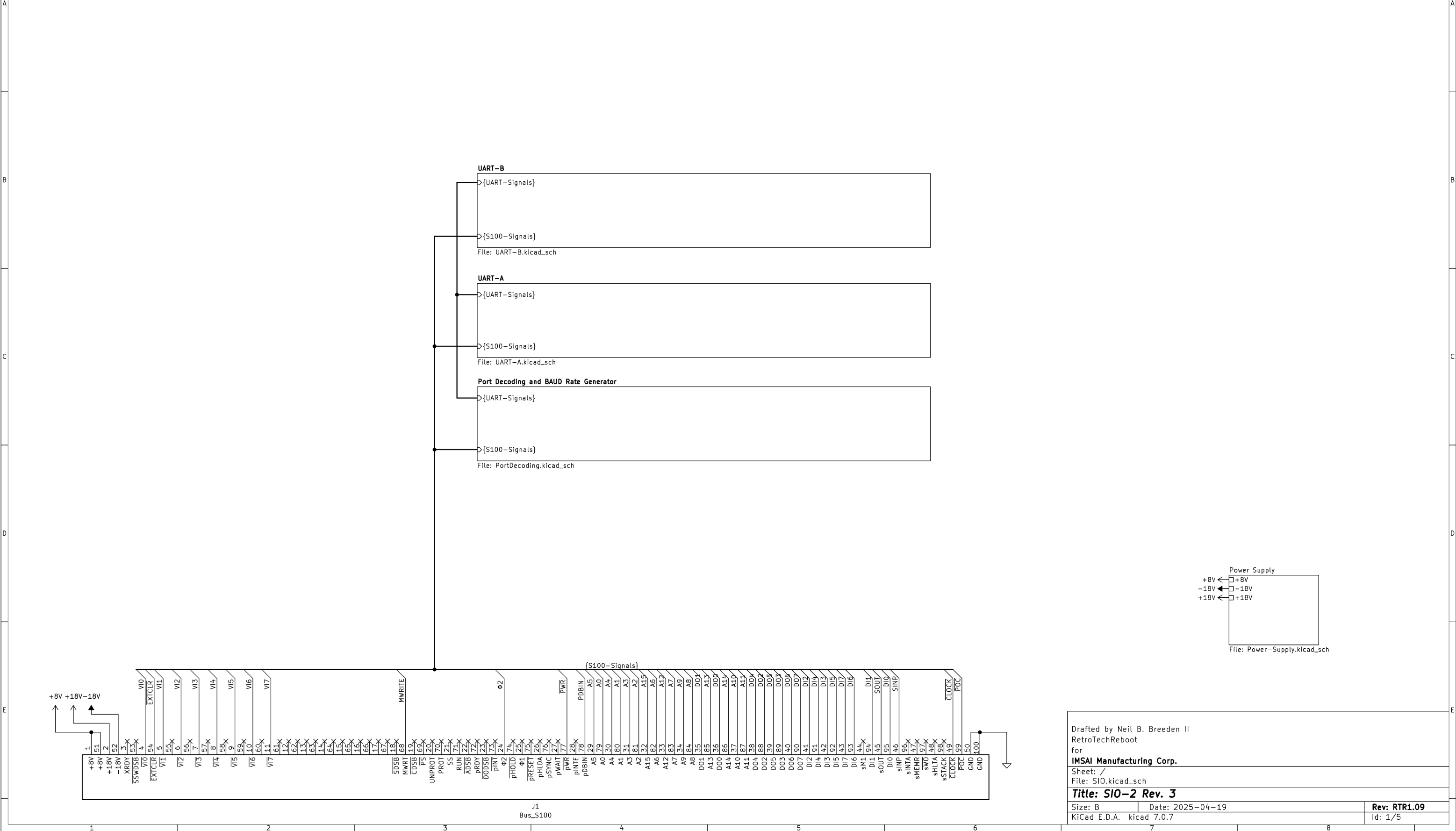
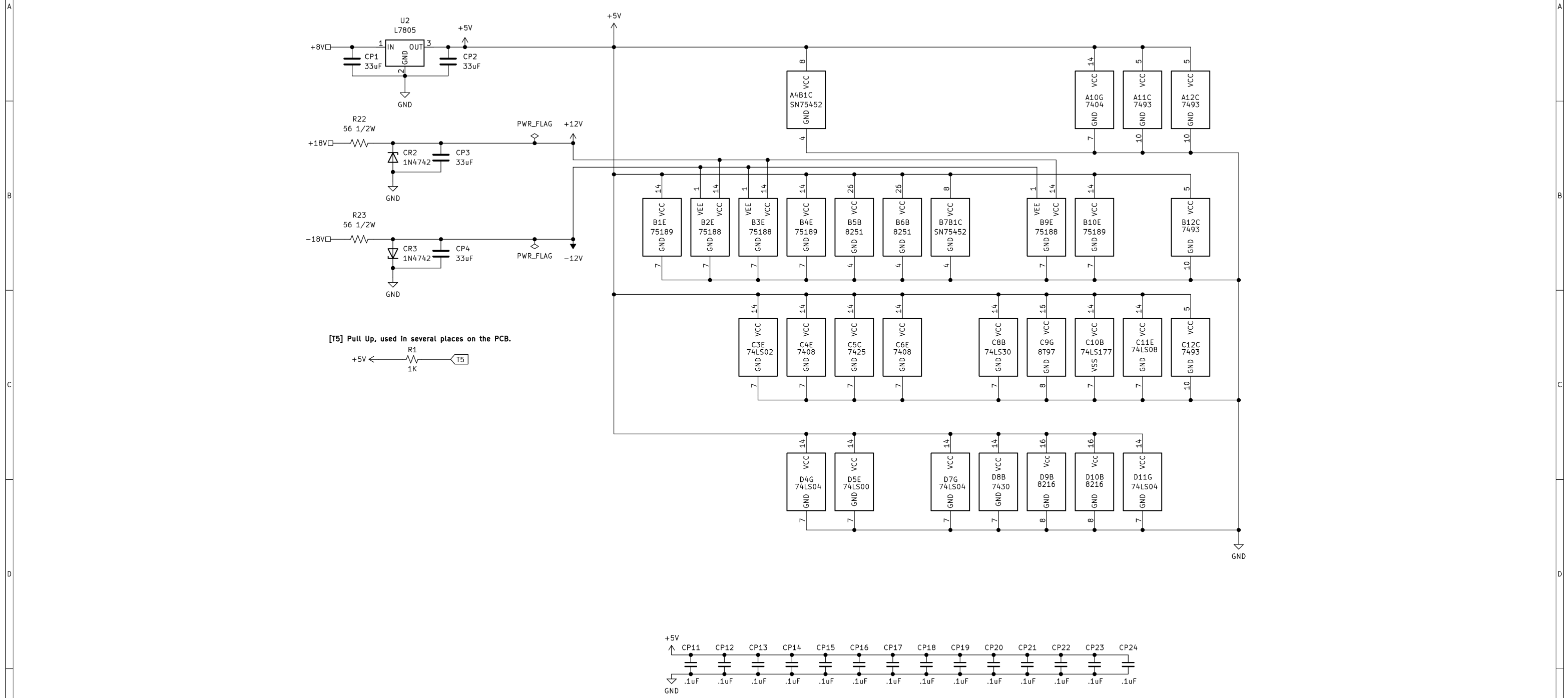
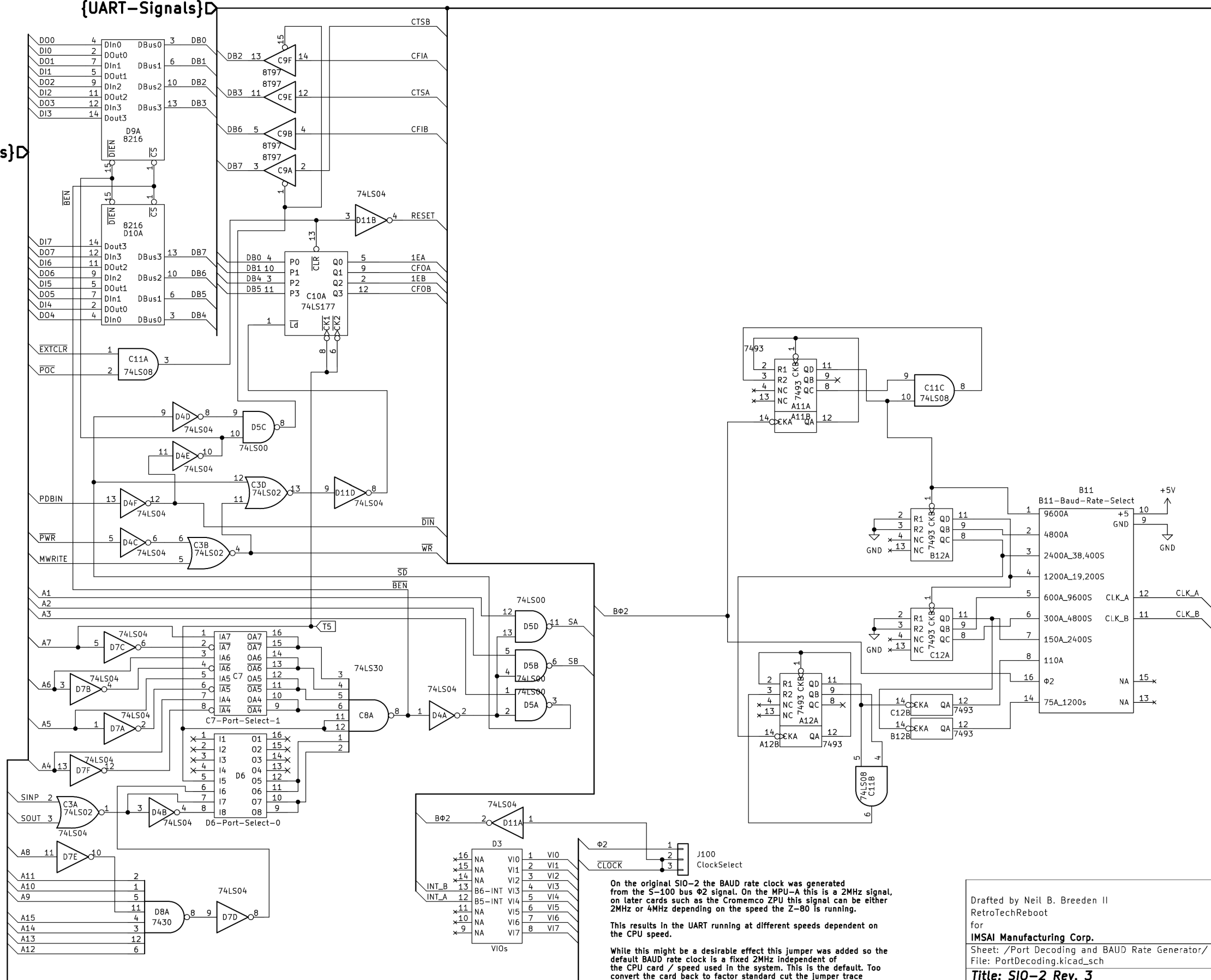




Pinout table for J1 (Bus_S100):

1	+BV	SDSB	UNPROT	02	pHOLD	A0	D01	sINP	POC	50
51	+BV	MWRT	PROT	01	PRESET	A4	D04	sMEMR	GND	100
2	+1BV	CDSB	55	01	PHDA	A8	D08	97X		
52	+1BV	19	21X	25	pTNC	A12	D12	98X		
3	-1BV	69	22X	26	pWAIT	A16	D16	44X		
53	XRDY	15	23X	27	pPINT	A20	D20	45		
4	SSWDSB	16	24X	28	pPINT	A24	D24	46		
54	V10	17	25X	29	pPINT	A28	D28	47		
55	EXTCLR	18	26X	30	pPINT	A32	D32	48		
56	V11	19	27X	31	pPINT	A36	D36	49		
57	V12	20	28X	32	pPINT	A40	D40	50		
58	V13	21	29X	33	pPINT	A44	D44	51		
59	V14	22	30X	34	pPINT	A48	D48	52		
60	V15	23	31X	35	pPINT	A52	D52	53		
61	V16	24	32X	36	pPINT	A56	D56	54		
62	V17	25	33X	37	pPINT	A60	D60	55		
63	V18	26	34X	38	pPINT	A64	D64	56		
64	V19	27	35X	39	pPINT	A68	D68	57		
65	V20	28	36X	40	pPINT	A72	D72	58		
66	V21	29	37X	41	pPINT	A76	D76	59		
67	V22	30	38X	42	pPINT	A80	D80	60		
68	V23	31	39X	43	pPINT	A84	D84	61		
69	V24	32	40X	44	pPINT	A88	D88	62		
70	V25	33	41X	45	pPINT	A92	D92	63		
71	V26	34	42X	46	pPINT	A96	D96	64		
72	V27	35	43X	47	pPINT	A100	D100	65		
73	V28	36	44X	48	pPINT	A104	D104	66		
74	V29	37	45X	49	pPINT	A108	D108	67		
75	V30	38	46X	50	pPINT	A112	D112	68		
76	V31	39	47X	51	pPINT	A116	D116	69		
77	V32	40	48X	52	pPINT	A120	D120	70		
78	V33	41	49X	53	pPINT	A124	D124	71		
79	V34	42	50X	54	pPINT	A128	D128	72		
80	V35	43	51X	55	pPINT	A132	D132	73		
81	V36	44	52X	56	pPINT	A136	D136	74		
82	V37	45	53X	57	pPINT	A140	D140	75		
83	V38	46	54X	58	pPINT	A144	D144	76		
84	V39	47	55X	59	pPINT	A148	D148	77		
85	V40	48	60X	60	pPINT	A152	D152	78		
86	V41	49	61X	61	pPINT	A156	D156	79		
87	V42	50	62X	62	pPINT	A160	D160	80		
88	V43	51	63X	63	pPINT	A164	D164	81		
89	V44	52	64X	64	pPINT	A168	D168	82		
90	V45	53	65X	65	pPINT	A172	D172	83		
91	V46	54	66X	66	pPINT	A176	D176	84		
92	V47	55	67X	67	pPINT	A180	D180	85		
93	V48	56	68X	68	pPINT	A184	D184	86		
94	V49	57	69X	69	pPINT	A188	D188	87		
95	V50	58	70X	70	pPINT	A192	D192	88		
96	V51	59	71X	71	pPINT	A196	D196	89		
97	V52	60	72X	72	pPINT	A200	D200	90		
98	V53	61								





Note that S-100 Pin 3 $\overline{\text{CLOCK}}$ is defined to be a fixed 2MHz clock.

Unused Gates

The diagram shows seven unused gates in the 74181 ALU, each with its inputs and outputs marked with an 'X' to indicate they are not connected. The gates are:

- D11C (74LS04):** An inverter with input 5 and output 6.
- D11E (74LS04):** An inverter with input 11 and output 10.
- D11F (74LS04):** An inverter with input 13 and output 12.
- C11D (74LS08):** A 2-input AND gate with inputs 12 and 13, and output 11.
- C3C (74LS02):** A 2-input NOR gate with inputs 8 and 9, and output 10.
- C9C (8T97):** An inverter with input 6 and output 7.
- C9D (8T97):** An inverter with input 10 and output 9.

