IMSAI ECO 25-0001

Engineering Change Order for: SIO 2 Rev-3 AR-2.1

Summary

A BAUD RATE source clock jumper block has been added to the AR-2.1 PCB to allow the board to use either the S-100 ϕ2 or $\overline{\text{CLOCK}}$ signal as the BAUD RATE Clock Source.

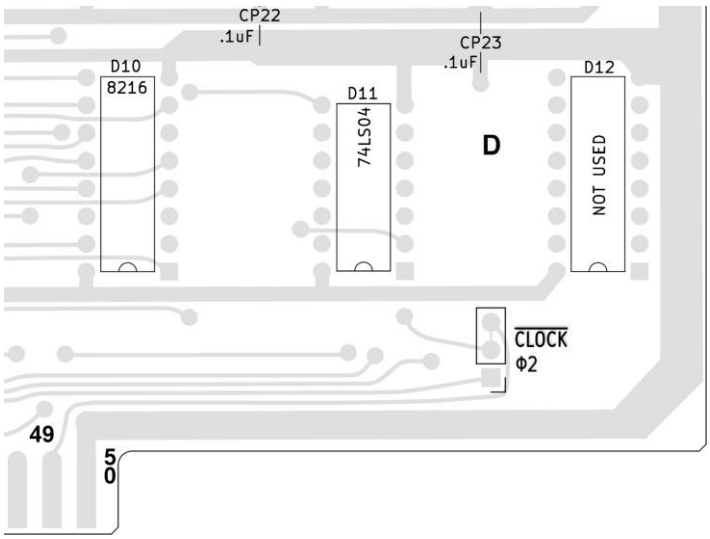
Details

Earlier SIO 2 PCBs used ϕ2 for the baud rate source clock as indicated in the original schematic diagram. For a 2MHz 8080 CPU such as the MPU-A board the use of ϕ2 worked as the SIO 2 design expects a 2MHz clock signal. On replacement CPU boards such as a 4MHz Z80 board the ϕ2 signal is 4MHz; this results in the UARTs running at 2× speed.

The S-100 $\overline{\text{CLOCK}}$ signal is a fixed 2MHz clock and is used by default by the SIO 2 AR-2.1 PCB. The user has the option to cut the trace between pins 2-3 then jumpering pins 1-2 to select ϕ2 as the clock source.

Notes

The default BAUD RATE Clock Source is the S-100 $\overline{\text{CLOCK}}$ signal which is specified to be a 2MHz TTL level clock.



Document Revision History

Revision	Date	Initial	Description
0	2025-04-28	NBB	Original.